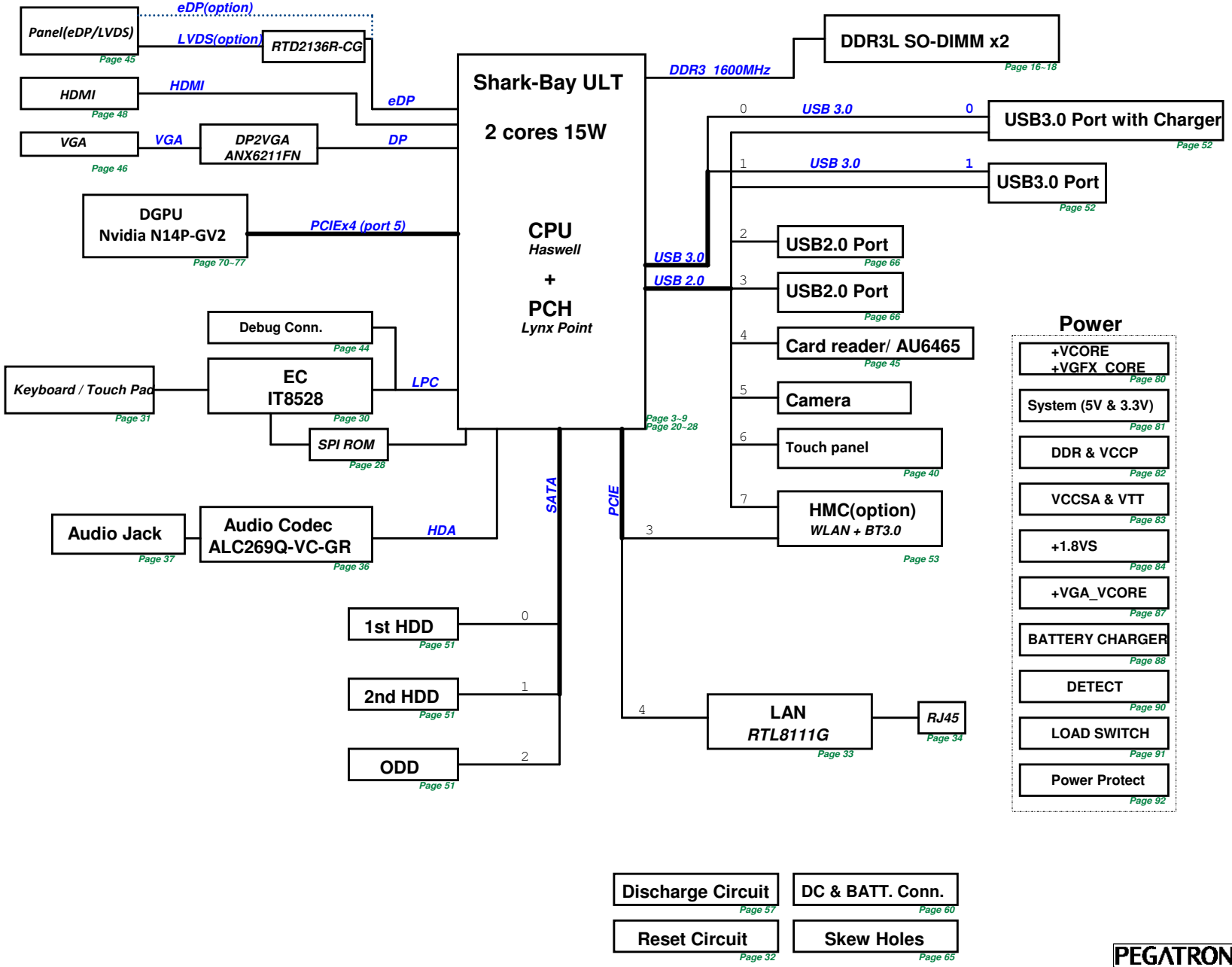
X750LB/LA with Shark Bay ULT

BLOCK DIAGRAM



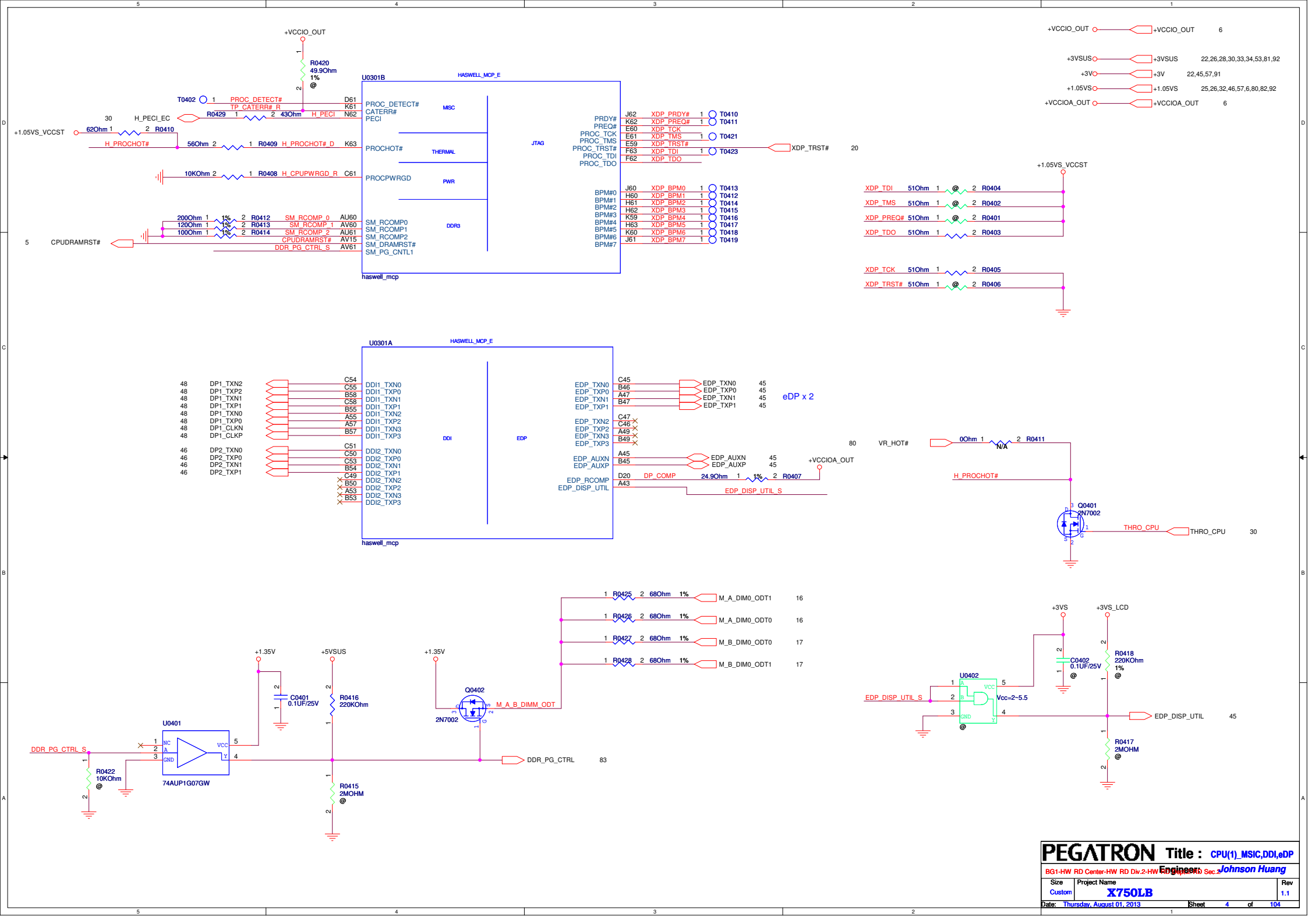
www.schematic-x.blogspot.com

PEGATRON Title : Block Diagram

Engineer: Johnson Huang

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 1 of 104



PEGATRON

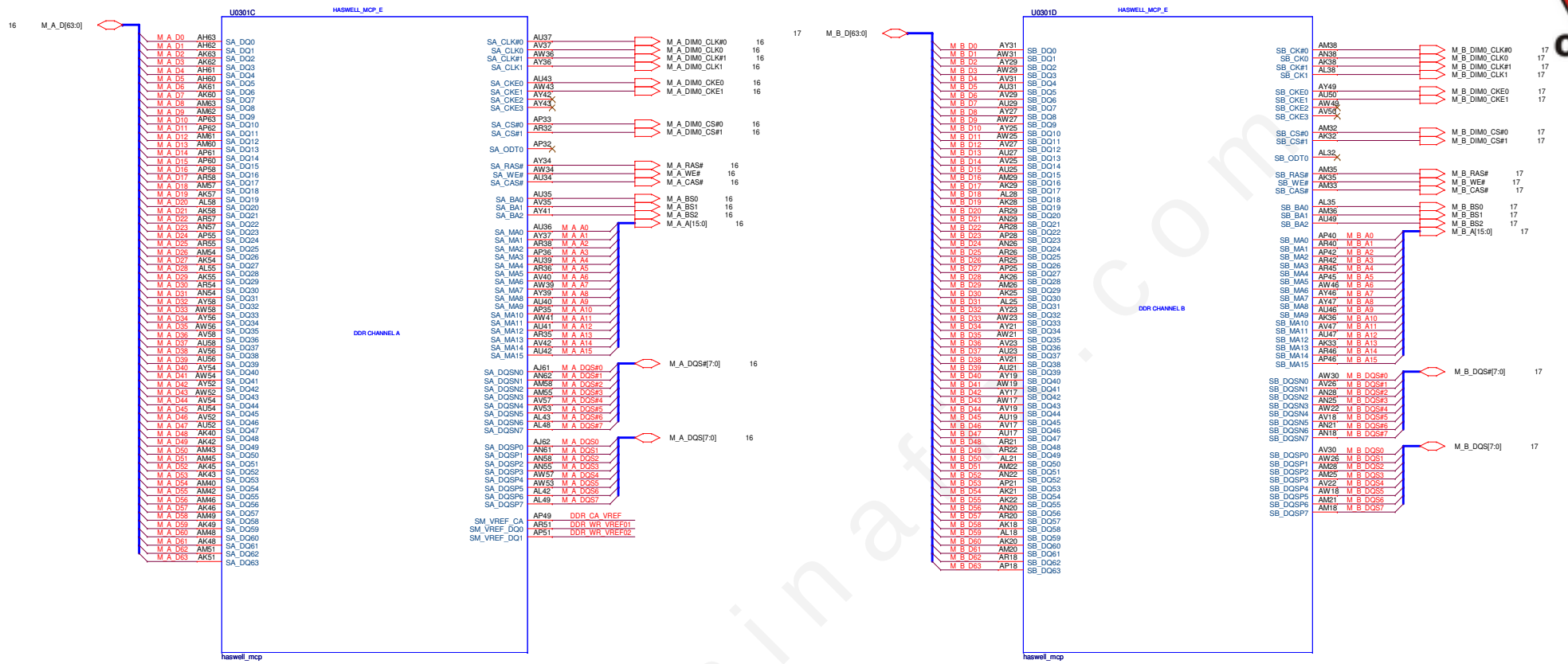
Title : CPU(1)_MSIC,DDI,eDP

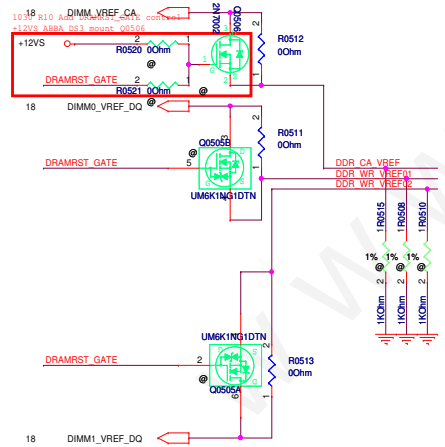
Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Sec.2

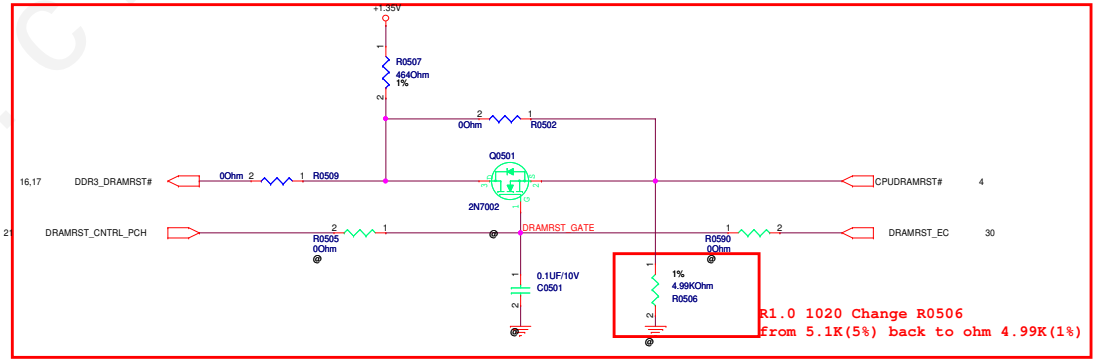
Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 4 of 104



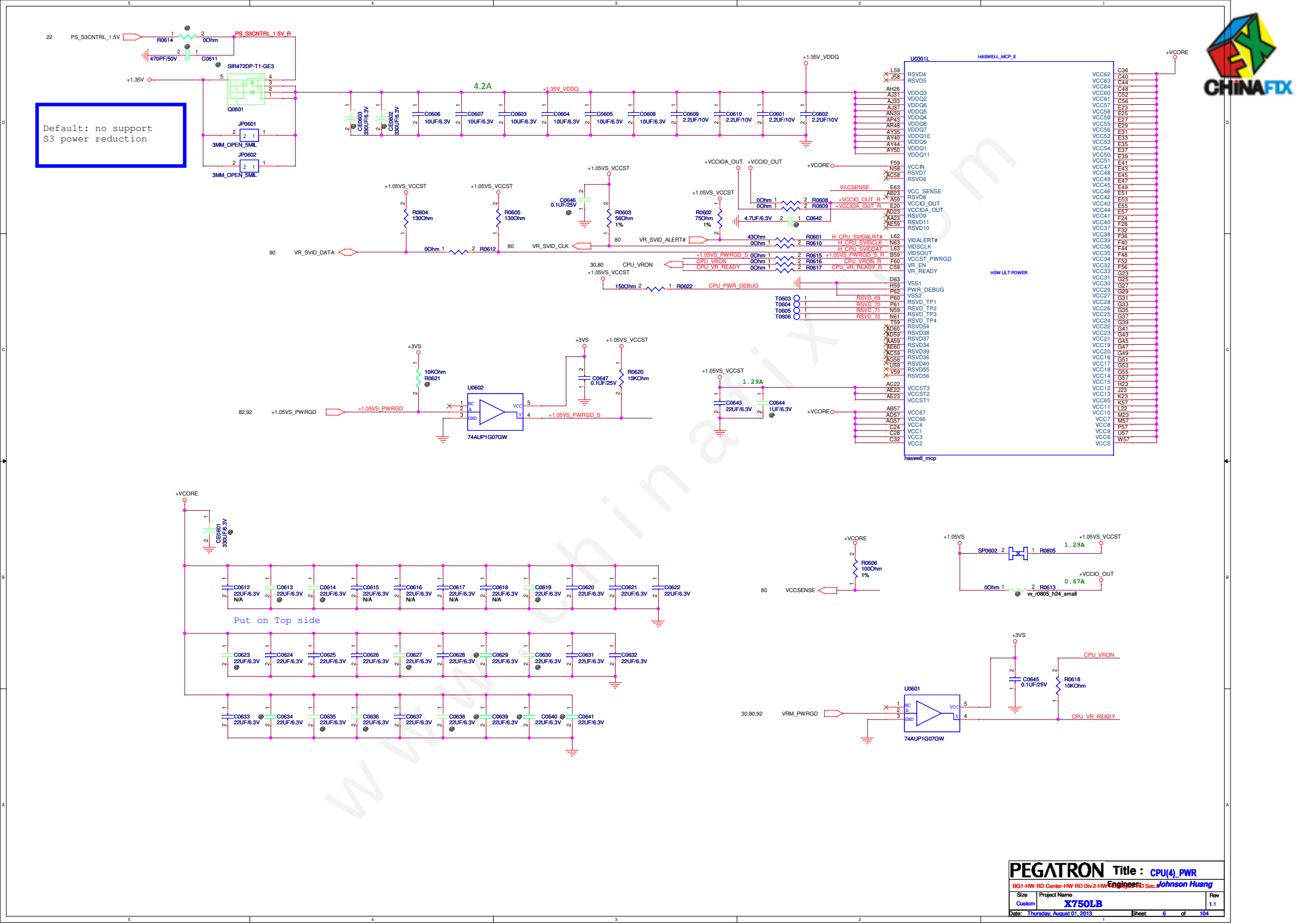


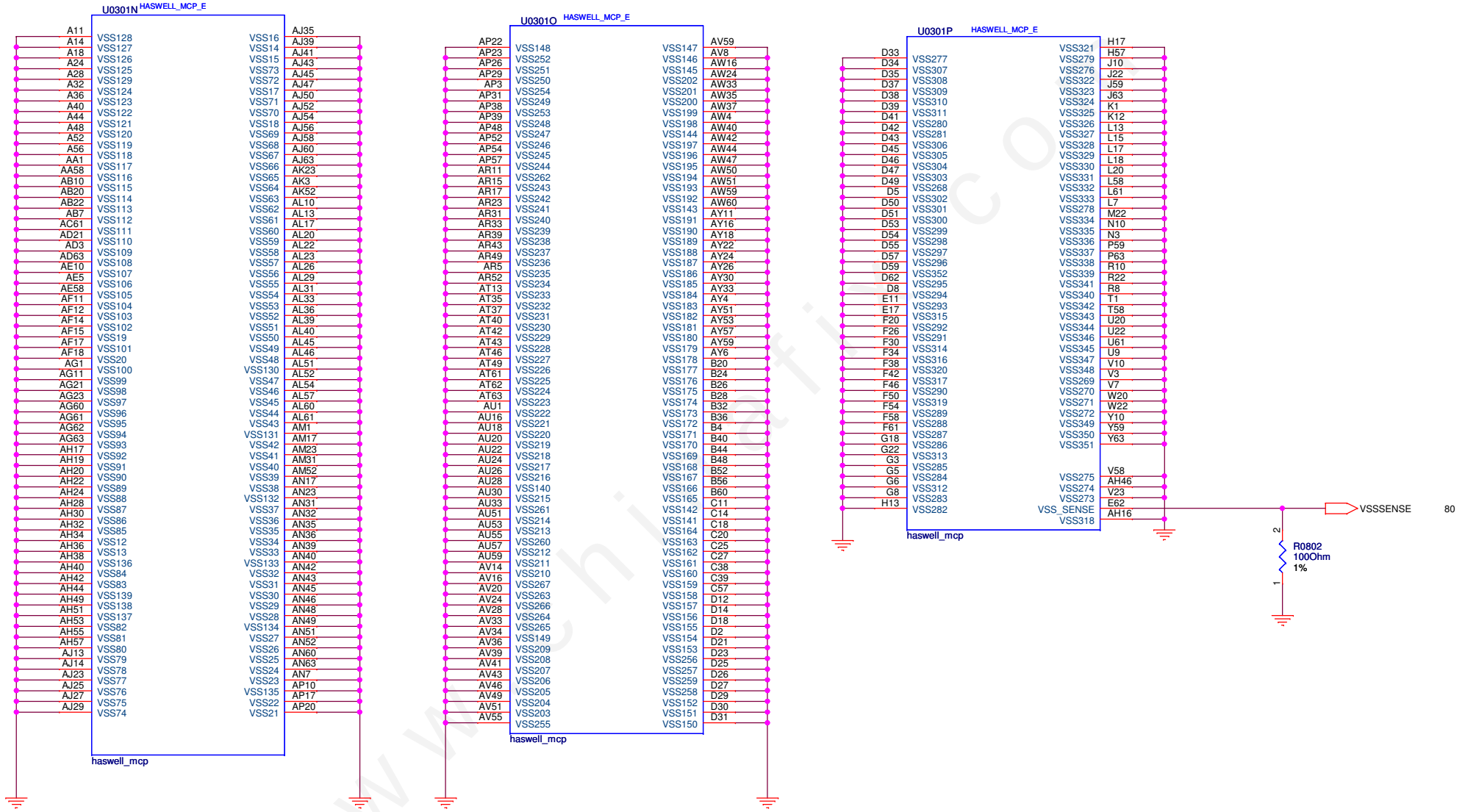
CPU driven VREF path is stuffed by default
CRB 0.7



PEGATRON	Title : CPU(2)_DDR3	
BG1-HW RD Center-HW RD Div.2-HW RD Sec.2	Engineer: Johnson Huang	
Size: C	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 5 of 104	

www.chinafix.com


Default: no support
S3 power reduction
PS_S3CNTRL_1.5V
PS_S3CNTRL_1.5V_R
R0614
0Ohm
C0611
470PF/50V
SIR472DP-T1-GE3
Q0601
+1.35V
JP0601
JP0602
3MM_OPEN_5MIL
4.2A
+1.35V_VDDQ
CE0603 330U/F/6.3V
CE0602 330U/F/6.3V
C0606 10UF/6.3V
C0607 10UF/6.3V
C0603 10UF/6.3V
C0604 10UF/6.3V
C0605 10UF/6.3V
C0608 10UF/6.3V
C0609 2.2UF/10V
C0610 2.2UF/10V
C0601 2.2UF/10V
C0602 2.2UF/10V
U0301L
HASWELL_MCP_E
haswell_mcp
HSW ULT POWER
+VCORE
+VCCIOA_OUT
+VCCIO_OUT
VCCSENSE
+1.05VS_VCCST
R0604 130Ohm
R0605 130Ohm
C0646 0.1UF/25V
R0603 56Ohm 1%
R0602 75Ohm 1%
C0642 4.7UF/6.3V
R0608
R0609
R0601 43Ohm
R0610 0Ohm
VR_SVID_DATA
VR_SVID_CLK
VR_SVID_ALERT#
H_CPU_SVIDALRT#
H_CPU_SVIDCLK
H_CPU_SVIDDAT
R0612 0Ohm
CPU_VRON
CPU_VR_READY
+1.05VS_PWRGD_S
R0615
R0616
R0617
VR_EN
VR_READY
CPU_PWR_DEBUG
R0622 150Ohm
T0603
T0604
T0605
T0606
RSVD_69
RSVD_70
RSVD_71
RSVD_72
+3VS
R0621 10KOhm
U0602
74AUP1G07GW
C0647 0.1UF/25V
R0620 10KOhm
1.29A
C0643 22UF/6.3V
C0644 1UF/6.3V
CE0601 330UF/6.3V
C0612 22UF/6.3V N/A
C0613 22UF/6.3V
C0614 22UF/6.3V
C0615 22UF/6.3V N/A
C0616 22UF/6.3V N/A
C0617 22UF/6.3V N/A
C0618 22UF/6.3V N/A
C0619 22UF/6.3V
C0620 22UF/6.3V
C0621 22UF/6.3V
C0622 22UF/6.3V
Put on Top side
C0623 22UF/6.3V
C0624 22UF/6.3V
C0625 22UF/6.3V
C0626 22UF/6.3V
C0627 22UF/6.3V
C0628 22UF/6.3V
C0629 22UF/6.3V
C0630 22UF/6.3V
C0631 22UF/6.3V
C0632 22UF/6.3V
C0633 22UF/6.3V
C0634 22UF/6.3V
C0635 22UF/6.3V
C0636 22UF/6.3V
C0637 22UF/6.3V
C0638 22UF/6.3V
C0639 22UF/6.3V
C0640 22UF/6.3V
C0641 22UF/6.3V
R0606 100Ohm 1%
SP0602
R0805
1.29A
0.67A
R0613
vx_r0805_h24_small
U0601
74AUP1G07GW
C0645 0.1UF/25V
R0618 10KOhm
CPU_VRON
CPU_VR_READY
VRM_PWRGD
+1.05VS_PWRGD
PEGATRON
Title : CPU(4)_PWR
Engineer: Johnson Huang
Size Custom
Project Name X750LB
Rev 1.1
Date: Thursday, August 01, 2013
Sheet 6 of 104

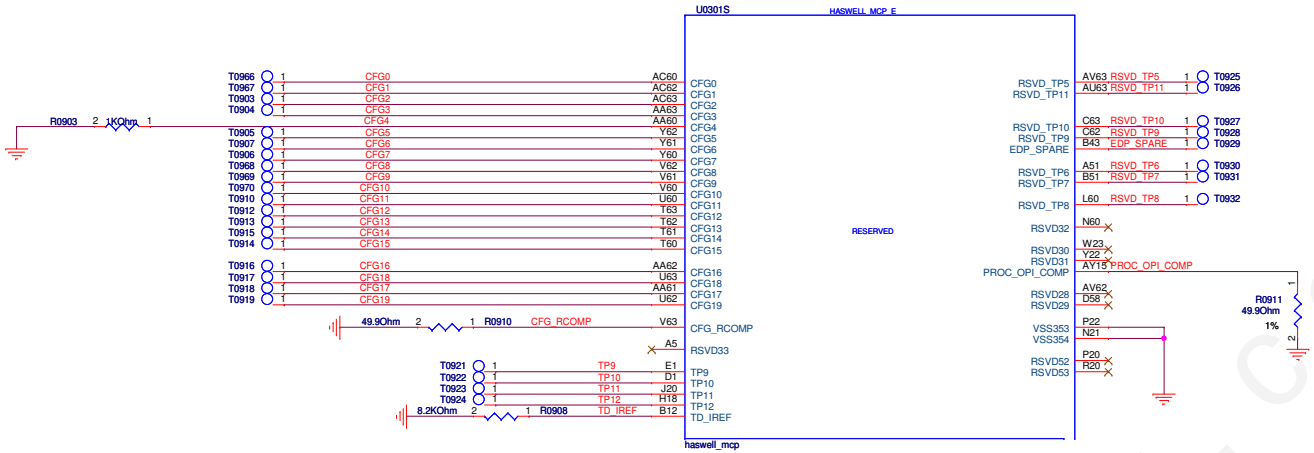


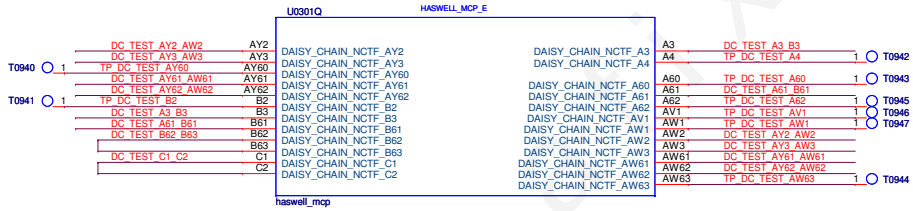
PEGATRON Title : CPU(3)_CFG,RSVD,GND

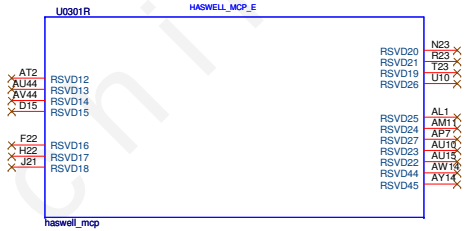
BG1-HW RD Center-HW RD Div.2-HW RD Sect.2-HW RD Sect.3 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 8 of 104







www.chinafdx.com

PEGATRON

Title: CPU(3)_CFG,RSVD,GND

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Sec.2

Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 9 of 104

+1.35V → +1.35V 18,4,5,57,6,83
+1.35V_DDR3 → +1.35V_DDR3 17,18
+0.675VS → +0.675VS 17,57,83
+3VS → +3VS 17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+V_VREF_CA_DIMM0 → +V_VREF_CA_DIMM0 18
+V_VREF_DQ_DIMM0 → +V_VREF_DQ_DIMM0 18

+1.35V — JP1601 — +1.35V_DDR3
3mm_open_5mil_m1m2

X750LB R1.0 Remove Ce1603

+1.35V_DDR3
Layout Note: Place these caps near SO DIMM 0
C1609 10UF/6.3V
C1610 10UF/6.3V
C1611 10UF/6.3V
C1612 @ 10UF/6.3V
C1613 @ 10UF/6.3V
C1620 10UF/6.3V

+0.675VS
C1616 1UF/6.3V
C1617 1UF/6.3V
C1618 1UF/6.3V @
C1619 1UF/6.3V @

X750LB R11 Change to reverse type

5 M_A_A[15:0]

J1601A

M_A_A0	98	A0	DQ0	5	M_A_D0
M_A_A1	97	A1	DQ1	7	M_A_D7
M_A_A2	96	A2	DQ2	15	M_A_D5
M_A_A3	95	A3	DQ3	17	M_A_D6
M_A_A4	92	A4	DQ4	4	M_A_D1
M_A_A5	91	A5	DQ5	6	M_A_D4
M_A_A6	90	A6	DQ6	16	M_A_D3
M_A_A7	86	A7	DQ7	18	M_A_D2
M_A_A8	89	A8	DQ8	21	M_A_D8
M_A_A9	85	A9	DQ9	23	M_A_D9
M_A_A10	107	A10/AP	DQ10	33	M_A_D13
M_A_A11	84	A11	DQ11	35	M_A_D15
M_A_A12	83	A12/BC#	DQ12	22	M_A_D10
M_A_A13	119	A13	DQ13	24	M_A_D12
M_A_A14	80	A14	DQ14	34	M_A_D11
M_A_A15	78	A15	DQ15	36	M_A_D14
			DQ16	39	M_A_D19
			DQ17	41	M_A_D18
			DQ18	51	M_A_D17
			DQ19	53	M_A_D16
			DQ20	40	M_A_D20
			DQ21	42	M_A_D21
			DQ22	50	M_A_D22
			DQ23	52	M_A_D23
			DQ24	57	M_A_D24
			DQ25	59	M_A_D30
			DQ26	67	M_A_D31
			DQ27	69	M_A_D26
			DQ28	56	M_A_D25
			DQ29	58	M_A_D29
			DQ30	68	M_A_D27
			DQ31	70	M_A_D28
			DQ32	129	M_A_D33
			DQ33	131	M_A_D32
			DQ34	141	M_A_D34
			DQ35	143	M_A_D37
			DQ36	130	M_A_D36
			DQ37	132	M_A_D38
			DQ38	140	M_A_D39
			DQ39	142	M_A_D35
			DQ40	147	M_A_D44
			DQ41	149	M_A_D45
			DQ42	157	M_A_D47
			DQ43	159	M_A_D46
			DQ44	146	M_A_D40
			DQ45	148	M_A_D41
			DQ46	158	M_A_D42
			DQ47	160	M_A_D43
			DQ48	163	M_A_D59
			DQ49	165	M_A_D58
			DQ50	175	M_A_D61
			DQ51	177	M_A_D56
			DQ52	164	M_A_D62
			DQ53	166	M_A_D63
			DQ54	174	M_A_D60
			DQ55	176	M_A_D57
			DQ56	181	M_A_D52
			DQ57	183	M_A_D51
			DQ58	191	M_A_D48
			DQ59	193	M_A_D49
			DQ60	180	M_A_D50
			DQ61	182	M_A_D53
			DQ62	192	M_A_D55
			DQ63	194	M_A_D54
		SCL	RESET#	30	DDR3_DRAMRST# 17,5
		SDA			

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

M_A_DIM0_CLK0 — C1621 10PF/50V @ — R1603 150Ohm 1% @
M_A_DIM0_CLK#0
M_A_DIM0_CLK1 — C1626 10PF/50V @ — R1604 150Ohm 1% @
M_A_DIM0_CLK#1
PLACE CLOSE TO SODIMM

5 M_A_DIM0_CLK1 → CK1 102
5 M_A_DIM0_CLK#1 → CK1# 104
5 M_A_DIM0_CLK0 → CK0 101
5 M_A_DIM0_CLK#0 → CK0# 103
5 M_A_DIM0_CS#1 → S1# 121
5 M_A_DIM0_CS#0 → S0# 114
4 M_A_DIM0_ODT1 → ODT1 120
4 M_A_DIM0_ODT0 → ODT0 116
5 M_A_WE# → WE# 113
5 M_A_RAS# → RAS# 110
5 M_A_CAS# → CAS# 115
5 M_A_BS2 → BA2 79
5 M_A_BS1 → BA1 108
5 M_A_BS0 → BA0 109
5 M_A_DIM0_CKE1 → CKE1 74
5 M_A_DIM0_CKE0 → CKE0 73

SMBus Slave Address: A0H
R1605 10KOhm 201
R1606 10KOhm 197
R1.10

5 M_A_DQS[7:0]
5 M_A_DQS#[7:0]

M_A_DQS6	188	DQS7	DQS7#	186	M_A_DQS#6
M_A_DQS7	171	DQS6	DQS6#	169	M_A_DQS#7
M_A_DQS5	154	DQS5	DQS5#	152	M_A_DQS#5
M_A_DQS4	137	DQS4	DQS4#	135	M_A_DQS#4
M_A_DQS3	64	DQS3	DQS3#	62	M_A_DQS#3
M_A_DQS2	47	DQS2	DQS2#	45	M_A_DQS#2
M_A_DQS1	29	DQS1	DQS1#	27	M_A_DQS#1
M_A_DQS0	12	DQS0	DQS0#	10	M_A_DQS#0

For RF
M_A_DIM0_CKE1
M_A_DIM0_CKE0
SMB_CLK_S_CHA
SMB_DAT_S_CHA
C1627 10PF/50V @
C1628 10PF/50V @
C1629 10PF/50V @
C1630 10PF/50V @

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)

M_A_DM0	187	DM7	DM6	170	M_A_DM1
M_A_DM2	153	DM5	DM4	136	M_A_DM3
M_A_DM4	63	DM3	DM2	46	M_A_DM5
M_A_DM6	28	DM1	DM0	11	M_A_DM7

17,28,31,45,53 SMB_CLK_S — SP1601 — R0402 SMB_CLK_S_CHA 202
17,28,31,45,53 SMB_DAT_S — SP1602 — R0402 SMB_DAT_S_CHA 200

DDR3_DIMM_204P
12V02GBRM003

H:4mm

X750LB R11 Change to reverse type

+1.35V_DDR3
C1605 0.1UF/16V
C1606 0.1UF/16V
C1607 0.1UF/16V
C1608 0.1UF/16V

Layout Note: Place these caps near SO DIMM 0

J1601B

		VDD1	VDD2	76	
		VDD3	VDD4	82	
		VDD5	VDD6	88	
		VDD7	VDD8	94	
		VDD9	VDD10	100	
		VDD11	VDD12	106	
		VDD13	VDD14	112	
		VDD15	VDD16	118	
		VDD17	VDD18	124	
		VSS1	VSS2	3	
		VSS3	VSS4	9	
		VSS5	VSS6	14	
		VSS7	VSS8	20	
		VSS9	VSS10	26	
		VSS11	VSS12	32	
		VSS13	VSS14	38	
		VSS15	VSS16	44	
		VSS17	VSS18	49	
		VSS19	VSS20	55	
		VSS21	VSS22	61	
		VSS23	VSS24	65	
		VSS25	VSS26	72	
		VSS27	VSS28	128	
		VSS29	VSS30	134	
		VSS31	VSS32	139	
		VSS33	VSS34	145	
		VSS35	VSS36	151	
		VSS37	VSS38	156	
		VSS39	VSS40	162	
		VSS41	VSS42	168	
		VSS43	VSS44	173	
		VSS45	VSS46	179	
		VSS47	VSS48	185	
		VSS49	VSS50	190	
		VSS51	VSS52	196	
			GND1	207	
T1601 1 PM_EXTTS#0_DIM_A	198	EVENT#	GND2	208	
Reserve	125	TEST			
			NP_NC1	205	
	77	NC1	NP_NC2	206	
	122	NC2			
			VTT1	203	+0.675VS
			VTT2	204	+3VS
	126	VREFCA			
	1	VREFDQ	VDDSPD	199	

DDR3_DIMM_204P
12V02GBRM003

+V_VREF_CA_DIMM0
C1624 2.2UF/10V @
C1623 0.1UF/16V

+V_VREF_DQ_DIMM0
C1622 2.2UF/10V @
C1625 0.1UF/16V

C1615 0.1UF/16V
C1614 2.2UF/10V @

PEGATRON Title : DDR3L(1)_SO-DIMM0
BG1_BU2 Engineer: Shiro_Lin
Size: Custom | Project Name: X750LB | Rev: 1.1
Date: Thursday, August 01, 2013 | Sheet 16 of 94

www.chinafix.com

+1.35V_DDR3 +1.35V_DDR3 16,18
+0.675VS +0.675VS 16,57,83
+3VS +3VS 16,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+V_VREF_CA_DIMM1 +V_VREF_CA_DIMM1 18
+V_VREF_DQ_DIMM1 +V_VREF_DQ_DIMM1 18

X750LB R1.0 Remove Ce1703

+1.35V_DDR3
Layout Note: Place these caps near SO DIMM 0
C1709 10UF/6.3V
C1710 10UF/6.3V
C1711 @ 10UF/6.3V
C1712 @ 10UF/6.3V
C1713 @ 10UF/6.3V
C1726 10UF/6.3V

+0.675VS
C1716 1UF/6.3V
C1717 1UF/6.3V
C1718 1UF/6.3V @
C1719 1UF/6.3V @

X750LB R11 Change to reverse type

5 M_B_A[15:0]
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15

J1701A
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15
BA2 BA1 BA0
CK1 CK1# CK0 CK0#
S1# S0#
ODT1 ODT0
WE# RAS# CAS#
CKE1 CKE0
SA1 SA0
DQS7 DQS#7 DQS6 DQS#6 DQS5 DQS#5 DQS4 DQS#4 DQS3 DQS#3 DQS2 DQS#2 DQS1 DQS#1 DQS0 DQS#0
DM7 DM6 DM5 DM4 DM3 DM2 DM1 DM0
SCL SDA
RESET#

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

0~7 8~15 32~39 40~47 24~31 56~63 16~23 48~55

M_B_D[63:0] 5
M_B_D1 M_B_D0 M_B_D6 M_B_D3 M_B_D5 M_B_D4 M_B_D7 M_B_D2 M_B_D12 M_B_D9 M_B_D10 M_B_D14 M_B_D13 M_B_D8 M_B_D15 M_B_D11 M_B_D33 M_B_D36 M_B_D38 M_B_D34 M_B_D37 M_B_D32 M_B_D39 M_B_D35 M_B_D44 M_B_D40 M_B_D42 M_B_D43 M_B_D45 M_B_D41 M_B_D47 M_B_D46 M_B_D29 M_B_D28 M_B_D26 M_B_D31 M_B_D24 M_B_D30 M_B_D27 M_B_D60 M_B_D56 M_B_D62 M_B_D63 M_B_D61 M_B_D58 M_B_D59 M_B_D57 M_B_D17 M_B_D16 M_B_D22 M_B_D23 M_B_D20 M_B_D21 M_B_D19 M_B_D18 M_B_D55 M_B_D51 M_B_D48 M_B_D53 M_B_D49 M_B_D52 M_B_D50 M_B_D54

M_B_DIM0_CLK0 M_B_DIM0_CLK#0 M_B_DIM0_CLK1 M_B_DIM0_CLK#1
C1720 10PF/50V @ 1% 150Ohm R1707 @
C1721 10PF/50V @ 1% 150Ohm R1708 @
PLACE CLOSE TO SODIMM

5 M_B_DIM0_CLK1
5 M_B_DIM0_CLK#1
5 M_B_DIM0_CLK0
5 M_B_DIM0_CLK#0

5 M_B_DIM0_CS#1
5 M_B_DIM0_CS#0
4 M_B_DIM0_ODT1
4 M_B_DIM0_ODT0
5 M_B_WE#
5 M_B_RAS#
5 M_B_CAS#
5 M_B_BS2
5 M_B_BS1
5 M_B_BS0
5 M_B_DIM0_CKE1
5 M_B_DIM0_CKE0

SMBus Slave Address: A4H
+3VS R1705 10KOhm R1706 10KOhm
R1.10

5 M_B_DQS[7:0]
5 M_B_DQS#[7:0]

For RF
M_B_DIM0_CKE1 M_B_DIM0_CKE0 SMB_CLK_S_CHB SMB_DAT_S_CHB
C1727 10PF/50V @
C1728 10PF/50V @
C1729 10PF/50V @
C1730 10PF/50V @

16,28,31,45,53 SMB_CLK_S
16,28,31,45,53 SMB_DAT_S
SP1701 2 1 R0402 SMB_CLK_S_CHB
SP1702 2 1 R0402 SMB_DAT_S_CHB

DDR3_DRAMRST# 16,5

DDR3_DIMM_204P
12V02GBRM004

H:8mm

X750LB R11 Change to reverse type

+1.35V_DDR3
C1705 0.1UF/16V
C1706 0.1UF/16V
C1707 0.1UF/16V
C1708 0.1UF/16V

Layout Note: Place these caps near SO DIMM 1

J1701B
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52
GND1 GND2
EVENT# TEST
NP_NC1 NP_NC2
NC1 NC2
VTT1 VTT2
VREFCA VREFDQ VDDSPD

T1701 1 PM_EXTTS#0_DIM_B
Reserve

DDR3_DIMM_204P
12V02GBRM004

+V_VREF_CA_DIMM1
C1724 2.2UF/10V @
C1723 0.1UF/16V

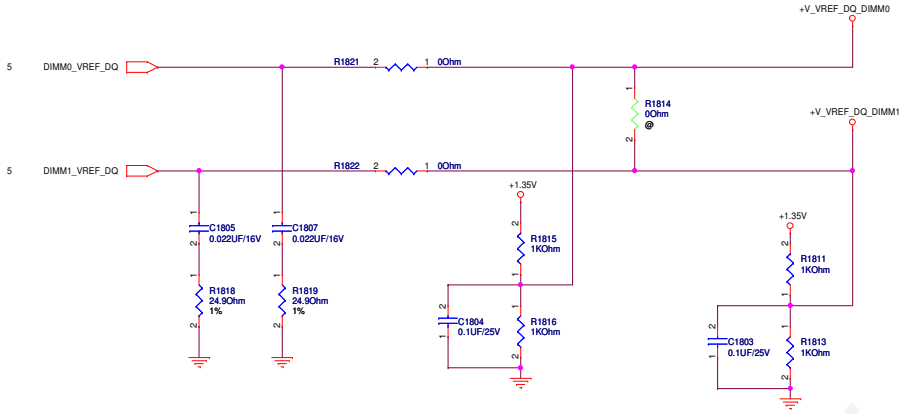
+V_VREF_DQ_DIMM1
C1722 2.2UF/10V @
C1725 0.1UF/16V

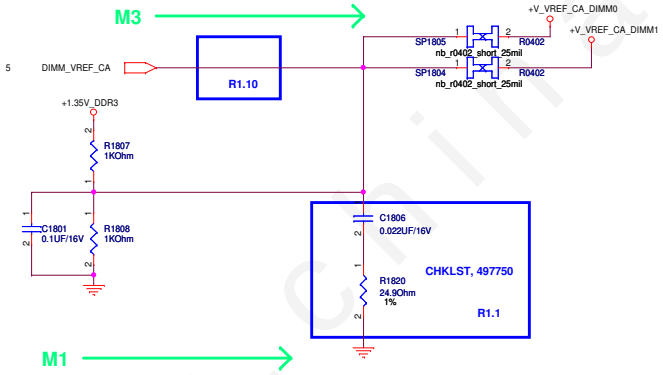
+0.675VS
+3VS
C1715 0.1UF/16V
C1714 2.2UF/10V @

www.chinafix.com

PEGATRON
Title : DDR3(2)_SO-DIMM1
BG1_BU2
Engineer: Shiro_Lin
Size: Custom
Project Name: X750LB
Rev: 1.1
Date: Thursday, August 01, 2013
Sheet 17 of 94

DDR3 Vref





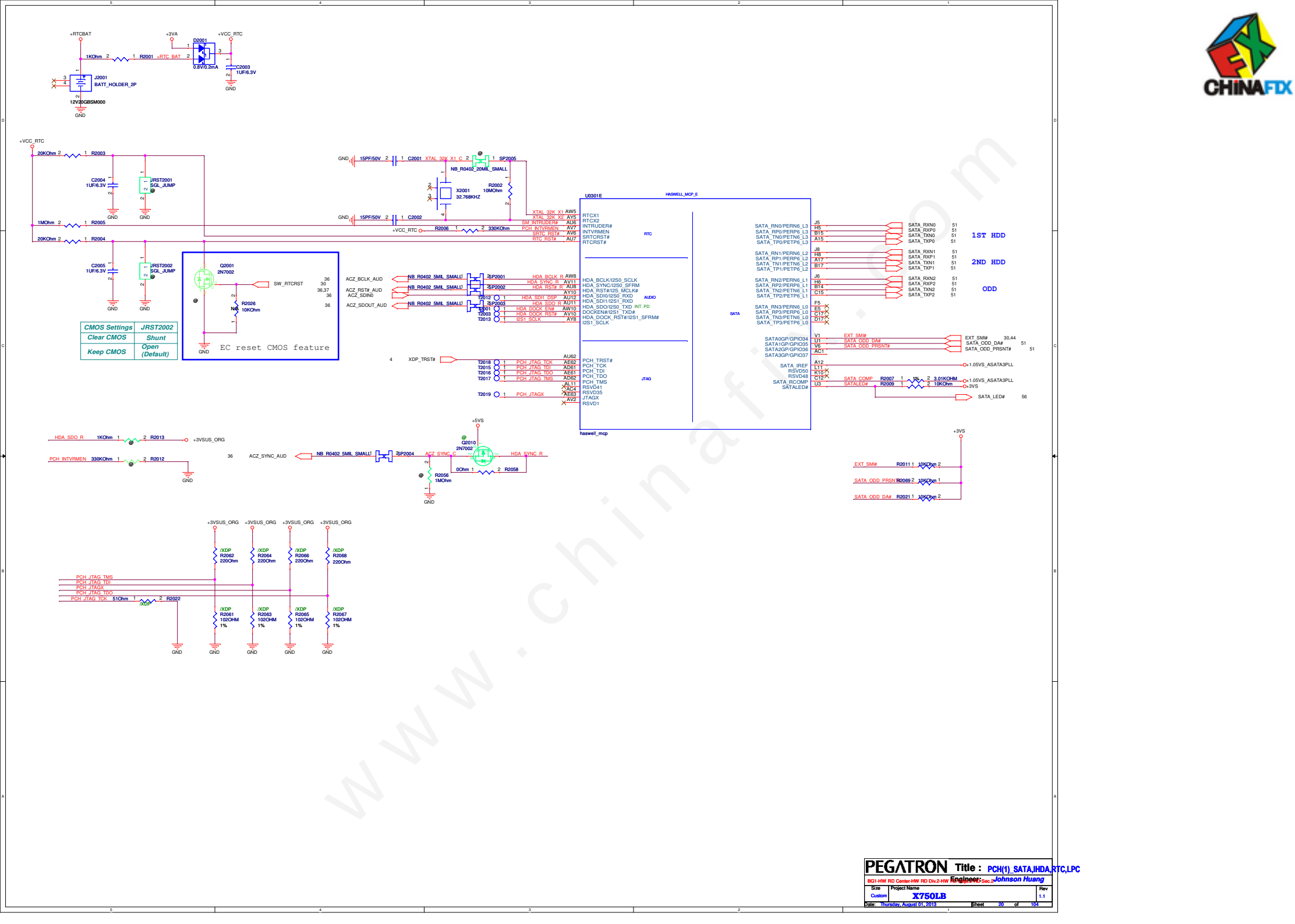
www.chinafix.com

PEGATRON Title : DDR3(3)_CA/DQ Voltage

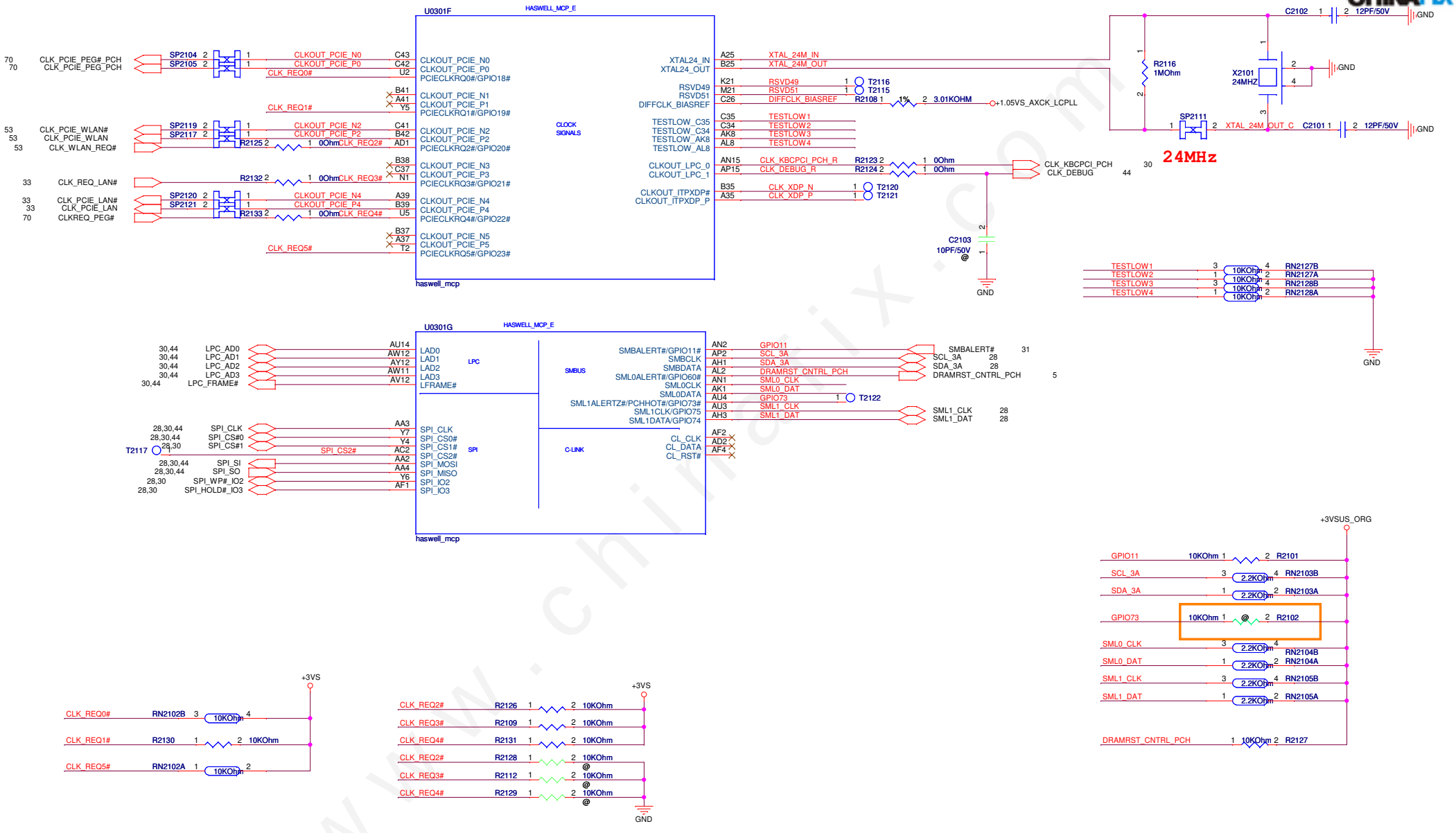
BG1-HW RD Center-HW RD Div.2-HW RD Sec.2 Engineer: Johnson Huang

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 18 of 100

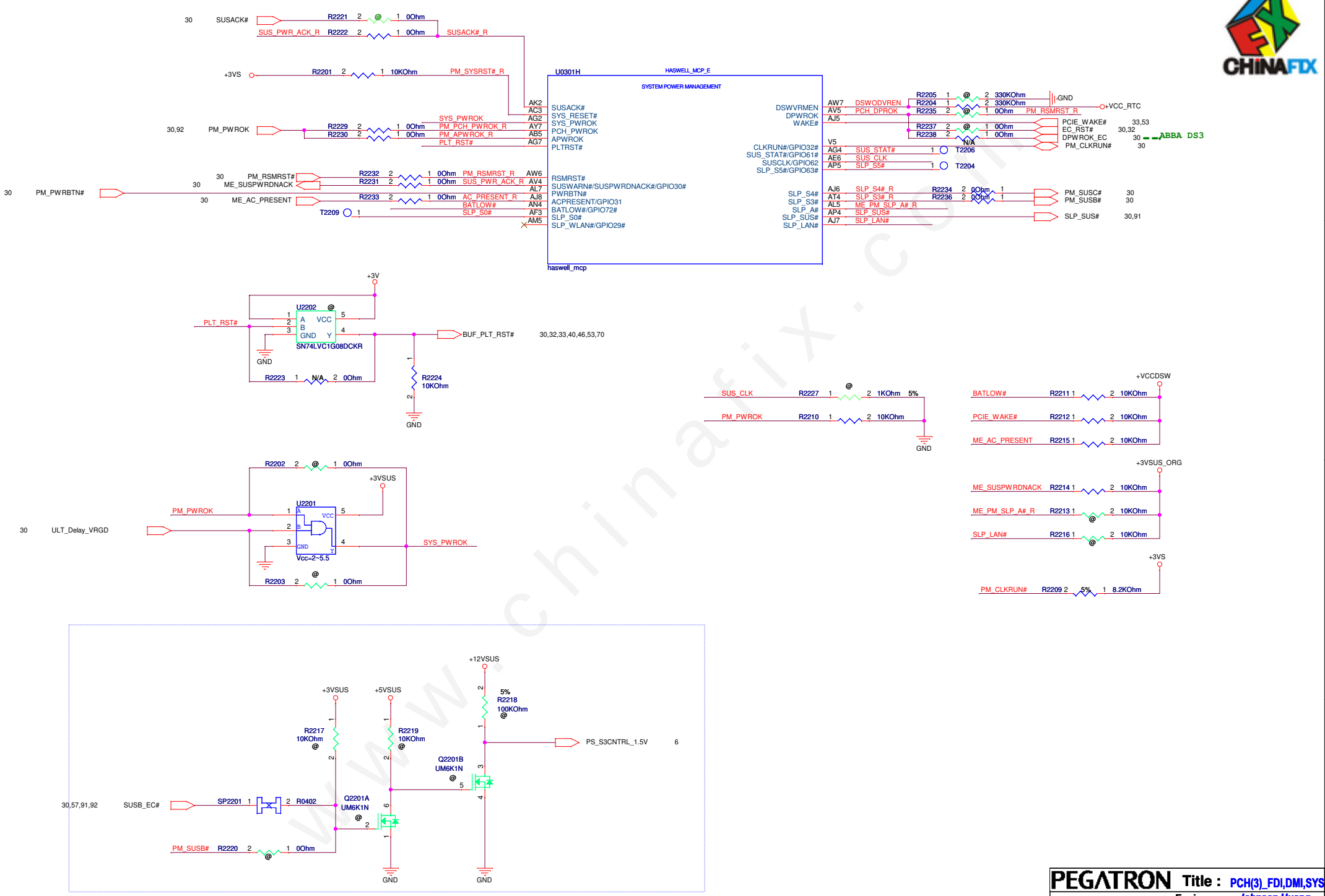


www.chinafix.com



www.chinafix.com

PEGATRON	Title : PCH(2)_PCIE,CLK,SME		
BG1-HW RD Center-HW RD Div.2-HW [illegible] Sec.2	Engineer: Johnson Huang		
Size: Custom	Project Name: X750LB		Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 21 of 104		



www.chinafix.com

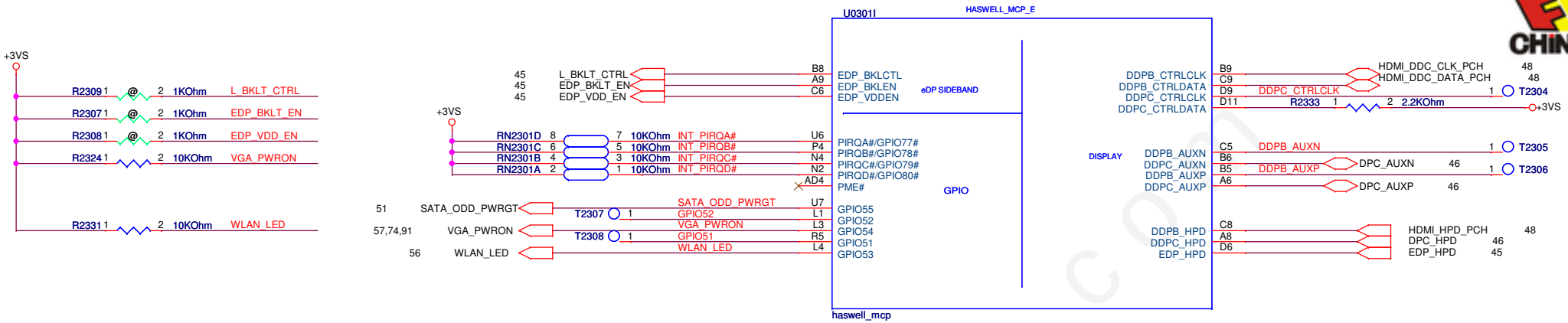
PEGATRON Title : PCH(3)_FDI,DMI,SYS P

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW [illegible] Sec.2

Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 22 of 104



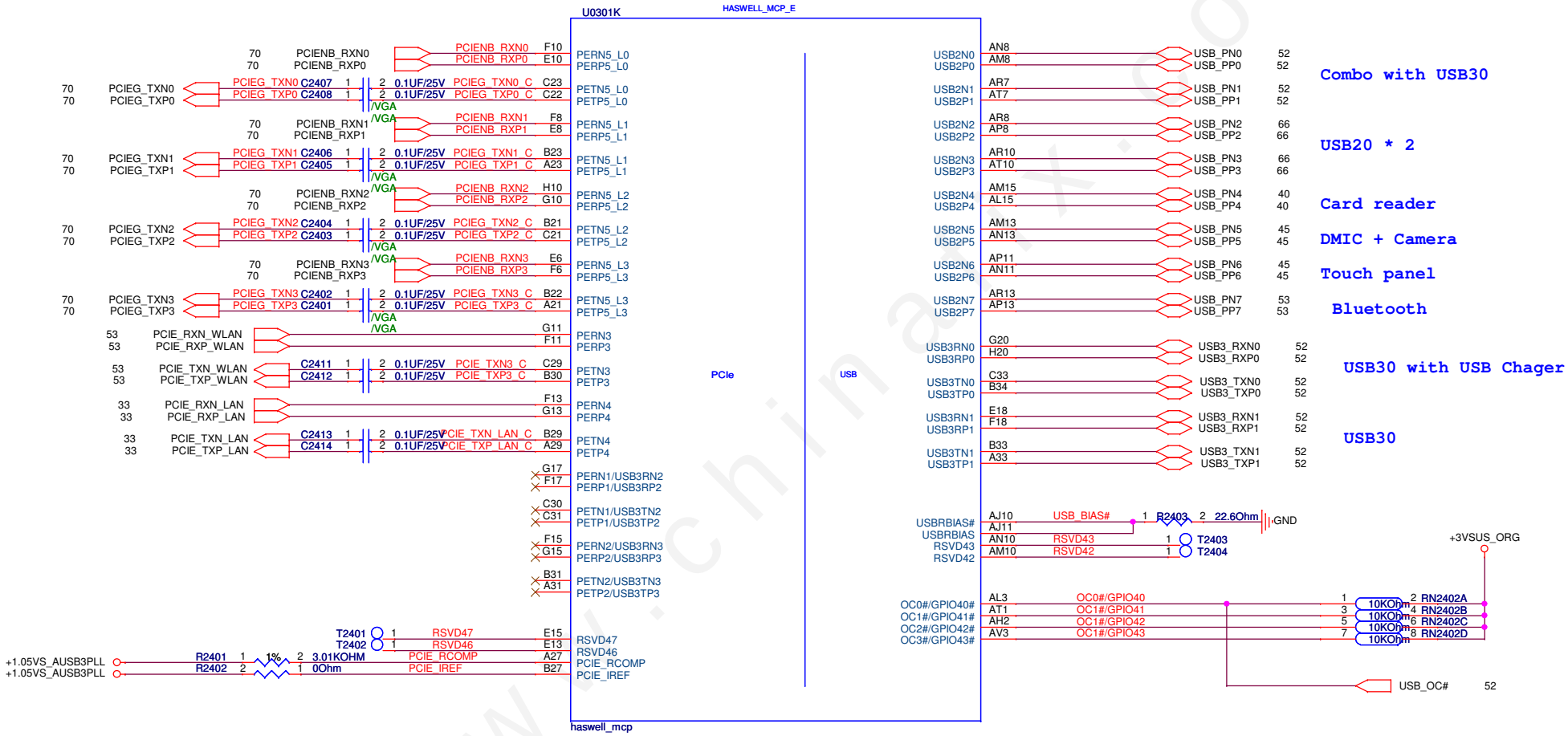
www.chinafix.com

PEGATRON Title : PCH(4)_DP,LVDS,CRT

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-HW RD Sec.2 Engineer: Johnson Huang

Size	Project Name	Rev
B	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 23 of 104

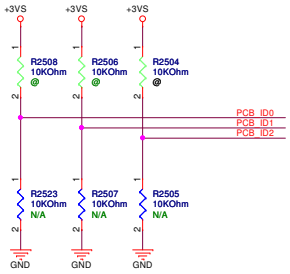


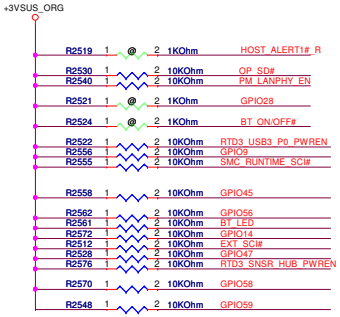
www.chinafix.com

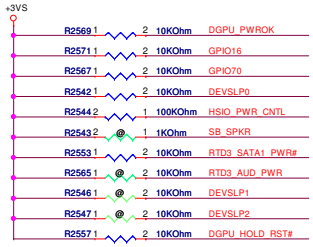
PEGATRON	Title : PCH(5)_PCI,NVRAM,USB		
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-HW RD Sect.2	Engineer: Johnson Huang		
Size: Custom	Project Name: X750LB	Rev: 1.1	
Date: Thursday, August 01, 2013	Sheet 24 of 104		

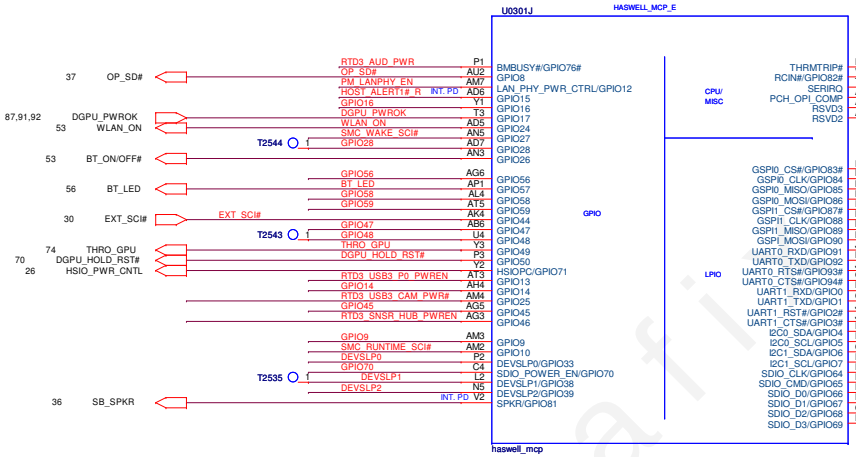
BIOS Rev. SKU

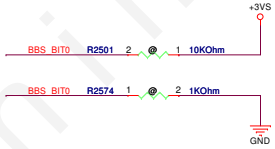
ID0	ID1	ID2	PCB Rev.
0	0	0	TBD
1	0	0	TBD
0	1	0	TBD
1	1	0	TBD
0	0	1	TBD
1	0	1	TBD
0	1	1	TBD
1	1	1	TBD

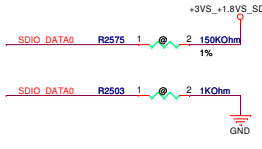


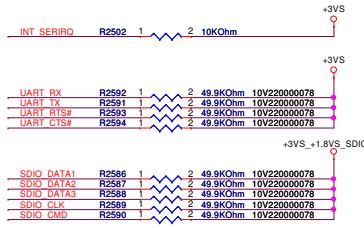


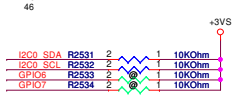


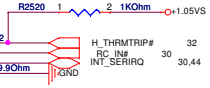












www.chinafix.com

PEGATRON

Title : PCH(6)_CPU,GPIO,MISC

Engineer: Johnson Huang

Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 25 of 104

Deep sleep mode: JP2603
Normal mode: JP2602

+3VSUS_DS3 +3VSUS_ORG
JP2603 1MM_OPEN_M1M2 /INTEL_DS3
+3VSUS
JP2602 1MM_OPEN_M1M2 /non_INTEL_DS3

20 +1.05VS_ASATA3PLL → +1.05VS_ASATA3PLL
24 +1.05VS_AUSB3PLL → +1.05VS_AUSB3PLL

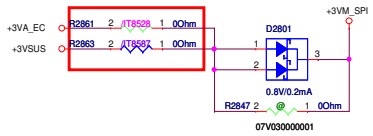
U0301M HASWELL_MCP_E
haswell_mcp

ABBA DS3
Refer to X750JB ABBA DS3 design
X750LB add R2618, R2619
X750LB change design to avoid RC delay

PEGATRON Title : PCH(8)_POWER,GND
Engineer: Johnson Huang
Size: Custom | Project Name: X750LB | Rev: 1.1
Date: Thursday, August 01, 2013 | Sheet 26 of 104

PCH SPI ROM

+3VA_EC reserved for share ROM



IT8587 mirror code
EC與SPI ROM的power plane需相同

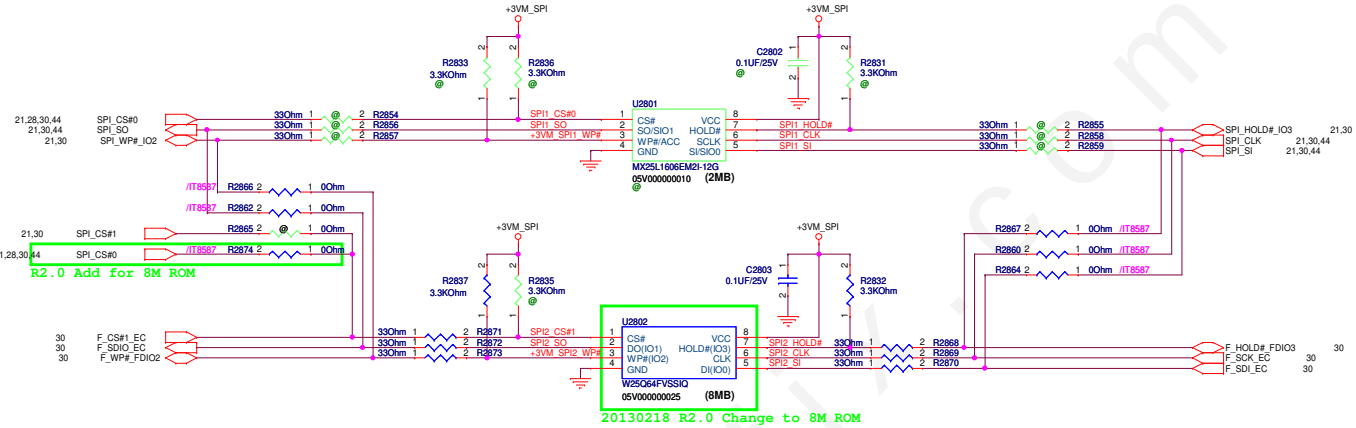
Option for Win8

Configuration1(Win 7)

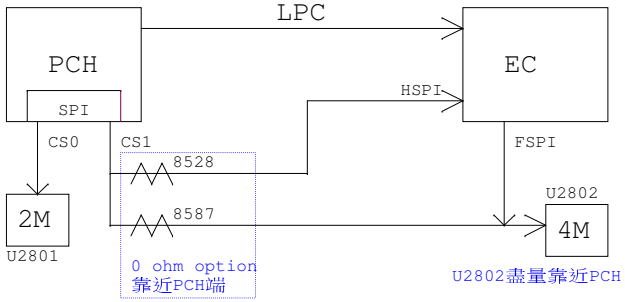
U2801	@	
U2802	@	
U2803	ME+BIOS+EC	4MB
ummount: R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802, R2869, R2870, R2868, D2802, U2801, R2835, R2836		

Configuration2(Win 8)

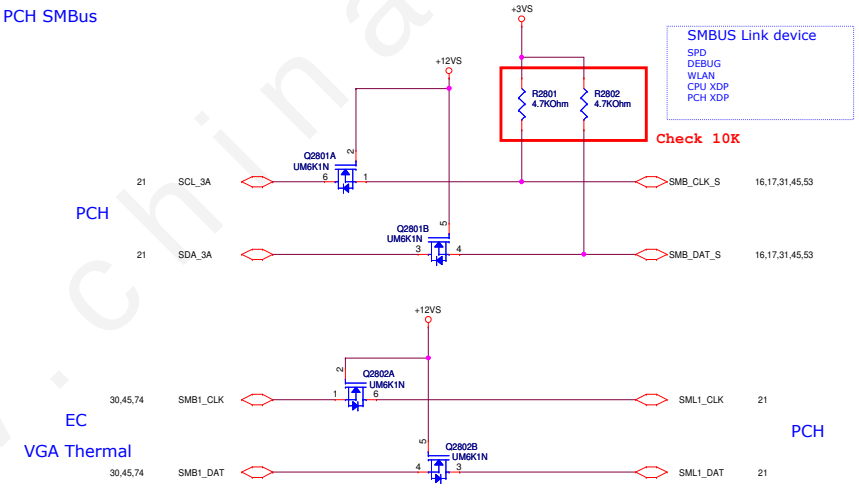
U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB
ummount: R2858, R2862, R2866, R2867, U2803		



EC co-lay 8528/8587
SPI Structure

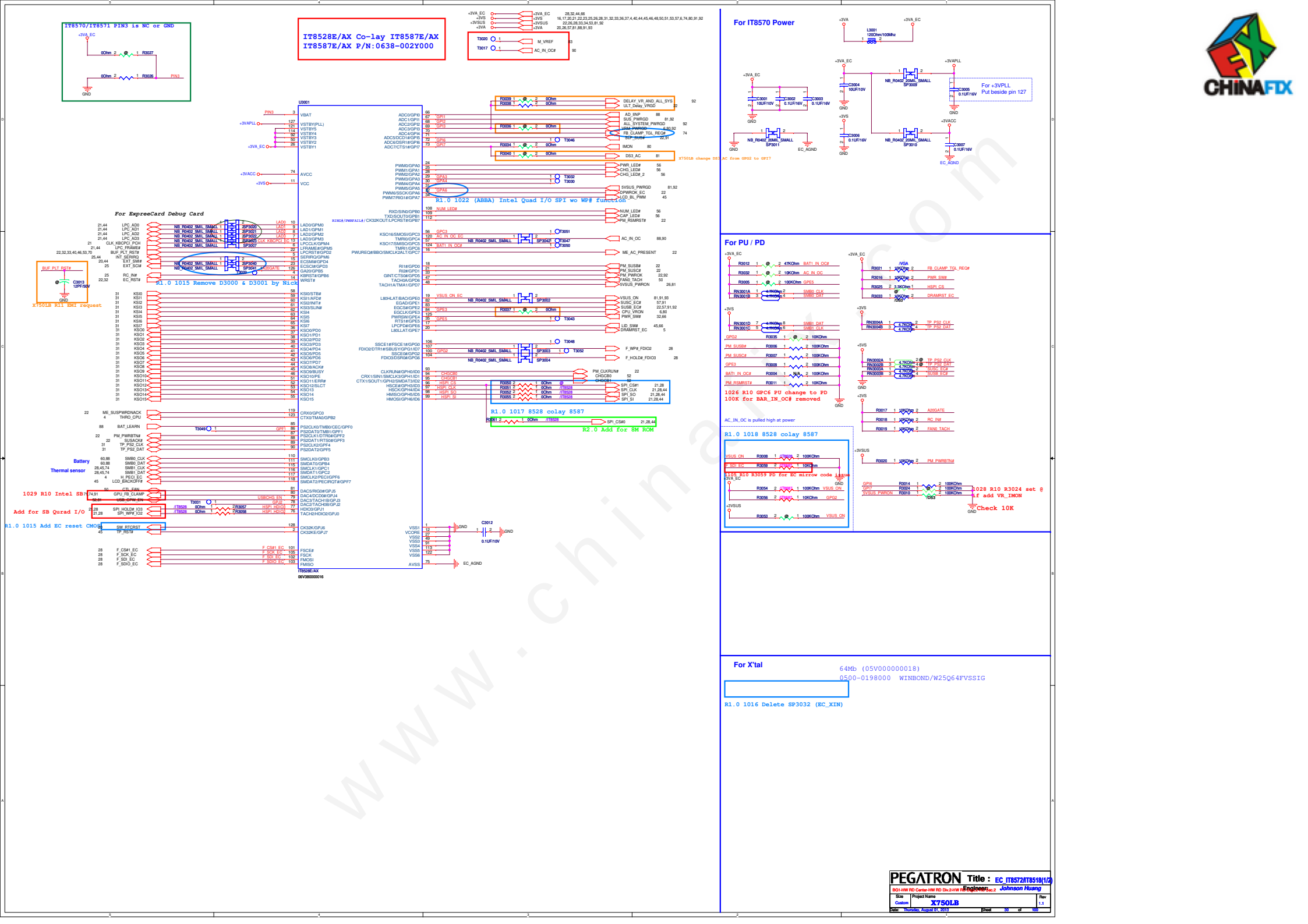


PCH SMBus

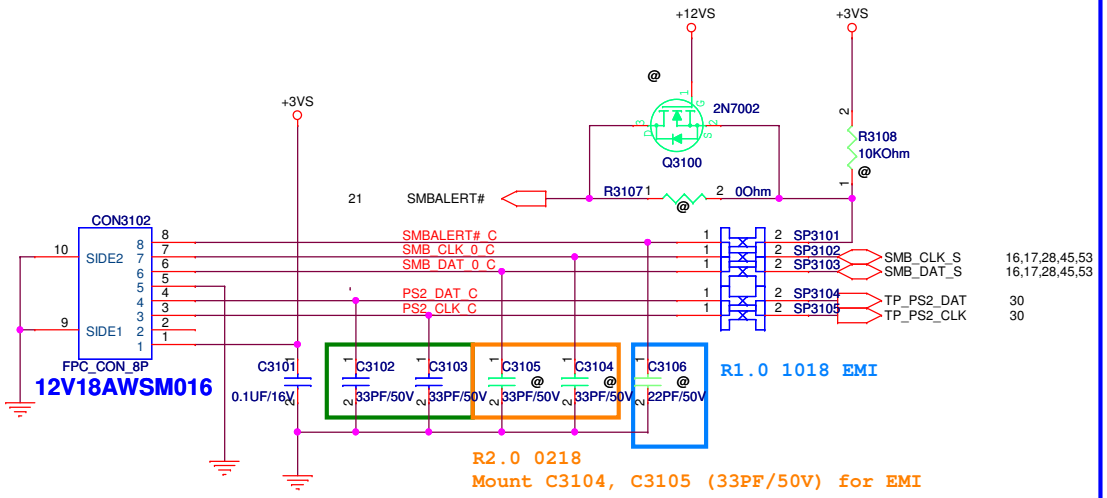


PEGATRON Title : PCH(9)_SPI,SMB
BG1_BU2 Engineer: Shiro_Lin
Size C | Project Name X750LB | Rev 1.1
Date: Thursday, August 01, 2013 | Sheet 28 of 100

www.chinafix.com

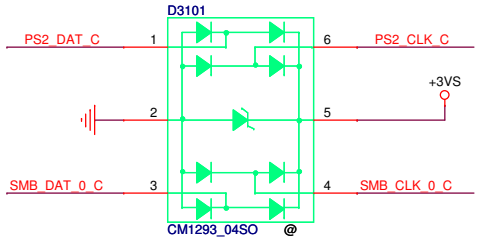

IT8570/IT8571 PIN3 is NC or GND
IT8528E/AX Co-lay IT8587E/AX
IT8587E/AX P/N:0638-002Y000
For IT8570 Power
For PU / PD
For X'tal
For ExpreeCard Debug Card
R1.0 1015 Remove D3000 & D3001 by Nick
R1.0 1022 (ABBA) Intel Quad I/O SPI wo WP# funct1.0
R1.0 1017 8528 colay 8587
R2.0 Add for 8M ROM
R1.0 1018 8528 colay 8587
1026 R10 GPC6 PU change to PD
100K for BAR_IN_OC# removed
1029 R10 Intel SB
Add for SB Quad I/O
R1.0 1015 Add EC reset CMOS
Battery
Thermal sensor
X750LB R11 EMI request
64Mb (05V000000018)
0500-0198000 WINBOND/W25Q64FVSSIG
R1.0 1016 Delete SP3032 (EC_XIN)
PEGATRON
Title : EC_IT8572/IT8518(1/2)
Engineer: Johnson Huang
X750LB

Touch Pad

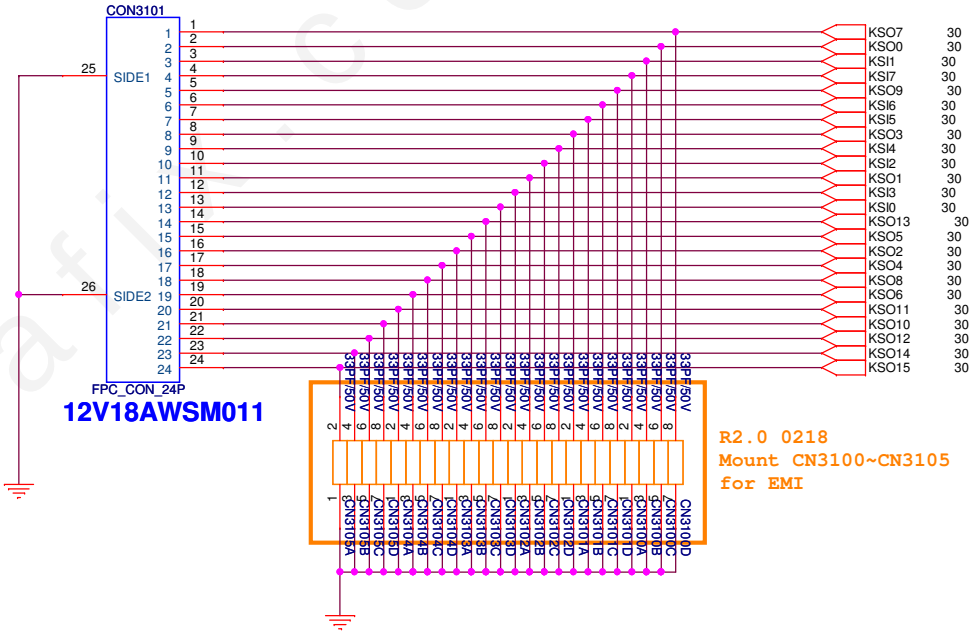


R2.0 0218
Mount C3104, C3105 (33PF/50V) for EMI

R1.2 0103 Change C3102, C3103
from 22pF to 33pF and Mount for EMI

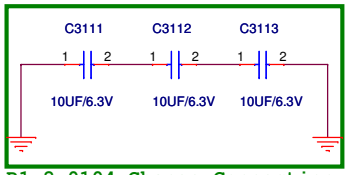


Keyboard



R2.0 0218
Mount CN3100~CN3105
for EMI

R1.2 0103 Add C3111, C3112, C3113 for EMI



R1.2 0104 Change Connection

+5VS +5VS 20,30,36,46,48,50,51,56,57,66,80,87,91

PEGATRON Title : EC_NPCE795L(2)KB, TP,I

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2 Engineer: Johnson Huang

Size	Project Name	Rev
B	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 31 of 100

www.chinafix.com

Thermal Policy

+3VS
+3VA_EC

+3VS
+3VA_EC

16,17,20,21,22,23,25,26,28,30,31,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
28,30,44,66

NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of
POR is less than 10us

74 VGA_THERM#

50,92 CPU_THERM#

SP3212
NB_R0402_5MIL_SMALL

+3VS
R3206
10KOhm

+3VA_EC
R3204 47KOhm
D3202
D3203

Q3202A
UM6K1N

Q3202B
UM6K1N

81,92 FORCE_OFF#

22,30,33,40,46,53,70 BUF_PLT_RST#

EC_RST# 22,30

C3201
1500PF/50V
1AV200000095

+1.05VS
R3202
330Ohm
Q3201
PMBS3904

25 H_THRMTRIP#

R1.2 0108 Add for EC 6s reset(mount)

+3VA_EC
R3205
N/A 1MOhm
R3207
1KOhm
N/A
R3203
1KOhm
UM6K1N
Q3203A
N/A
Q3203B
UM6K1N/A
N/A
C3202
10UF/6.3V

30,66 PWR_SW#

www.chinafix.com

PEGATRON

Title : RST_Reset Circuit

Engineer: Johnson Huang

Size	Project Name	Rev
A	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 32 of 100

+3VS +3VS 16,17,20,21,22,23,25,26,28,30,31,32,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92

+3VSUS +3VSUS 22,26,28,30,34,53,81,92

U3301A

34 L_TRDP0 → 1 MDIP0
34 L_TRDN0 → 2 MDIN0
34 L_TRDP1 → 4 MDIP1
34 L_TRDN1 → 5 MDIN1
34 L_TRDP2 → 6 MDIP2
34 L_TRDN2 → 7 MDIN2
34 L_TRDP3 → 9 MDIP3
34 L_TRDN3 → 10 MDIN3

AVDD33_1 11 DVDD33
AVDD33_2 32
VDDREG 23 DVDD33
REGOUT 24 REGOUT10

AVDD10_0 3 VDD10
AVDD10_1 8
AVDD10_2 30
DVDD10 22 VDD10

HSIP 13 PCIE_TXP_LAN 24
HSIN 14 PCIE_TXN_LAN 24
HSOP 17 PCIE_RXP3_LAN_C C3302 1 2 0.1UF/16V PCIE_RXP_LAN 24
HSON 18 PCIE_RXN3_LAN_C C3301 1 2 0.1UF/16V PCIE_RXN_LAN 24

REFCLK_P 15 CLK_PCIE_LAN 21
REFCLK_N 16 CLK_PCIE_LAN# 21

CKXTAL1 28 XTAL1
CKXTAL2 29 XTAL2

33 GND

RTL8111G-CG
02V0J0000024

200 mils

C3306 close to pins-- 24
C3307 to C3310 close to pins-- 3, 8, 22, 30
C3311 close to pins-- 22

200 mils

VDD10

REGOUT10 2 R3309 1 0Ohm

C3306 0.1UF/16V
C3307 0.1UF/16V
C3308 0.1UF/16V
C3309 0.1UF/16V
C3310 0.1UF/16V
C3311 1UF/6.3V

C3307 to C3311
Close To U3301

GND

C3316 to C3317 close to pins-- 11, 32

200 mils

+3VSUS 2 R3311 1 0Ohm DVDD33

C3316 0.1UF/16V
C3317 0.1UF/16V

GND

R1.0 1105

@
21 CLK_REQ_LAN# 1 R3304 2 0Ohm

R1.0 1031

+3VS
R3301 1 10KOhm 2 CLKREQB 12 CLKREQB
DVDD33 R3303 2 @ 1 10KOhm
22,53 PCIE_WAKE# 21 LANWAKEB

10K ohm close to Host side

ISOLATE 20 ISOLATEB

R1.2 1220 Set R3303 un-mount

+3VS
R3306 1KOhm
ISOLATE
R3307 15KOhm
GND

27 LED0
26 LED1/GPO
25 LED2

0,32,40,46,53,70 BUF_PLT_RST# 19 PERSTB
GND R3302 1 2.49KOhm 1% 2 31 RSET

R3302 close to pin31

C3301and C3302 Close to
U3301 pin17, pin18

@ C3321 18PF/50V GND
@ C3322 18PF/50V GND

R1.2 0103 Add C3321, C3322 for EA

X3302 25MHZ
XTAL1 XTAL2
C3304 12PF/50V GND
C3303 12PF/50V GND

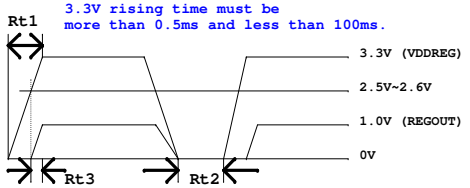
R1.2 1220 TXC recommend to adjust C3303,C3304=12pF

U3301B
34 GND1
35 GND2
36 GND3
37 GND4
38 GND5
39 GND6
40 GND7
41 GND8
GND

RTL8111G-CG
02V0J0000024

Power sequence

3.3V rising time must be
more than 0.5ms and less than 100ms.

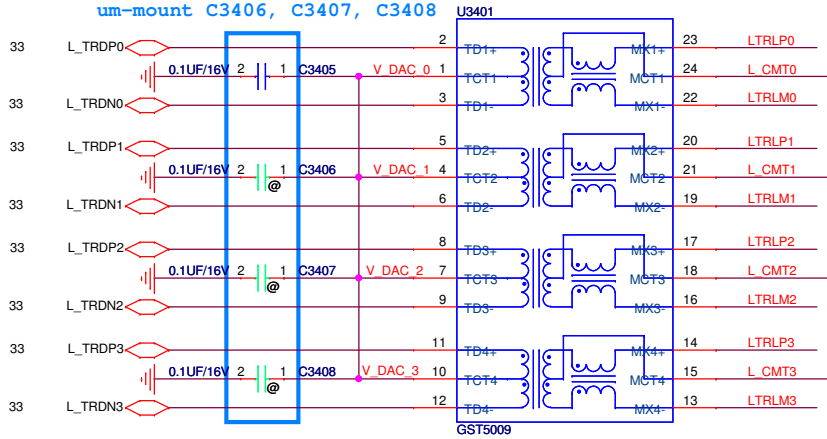


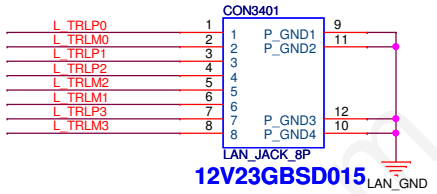
	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

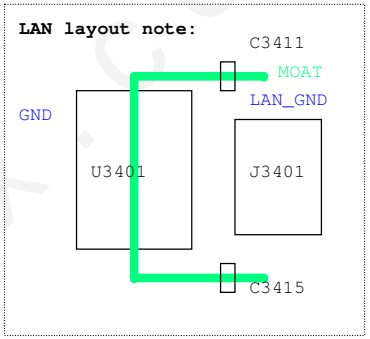
PEGATRON Title : Realtek RTL8111G
BG1-HW RD Center-HW RD Div.2-HW RD Dept.-HW RD Sec.2 Engineer: Johnson Huang
Size: Custom | Project Name: X750LB | Rev: 1.1
Date: Thursday, August 01, 2013 | Sheet 33 of 100

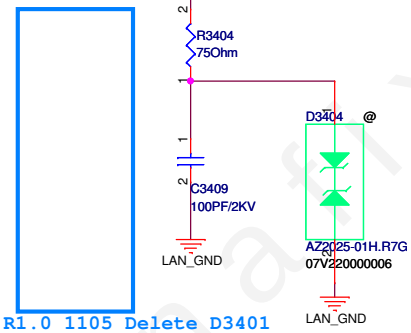
www.chinafix.com

R1.0 1026
um-mount C3406, C3407, C3408



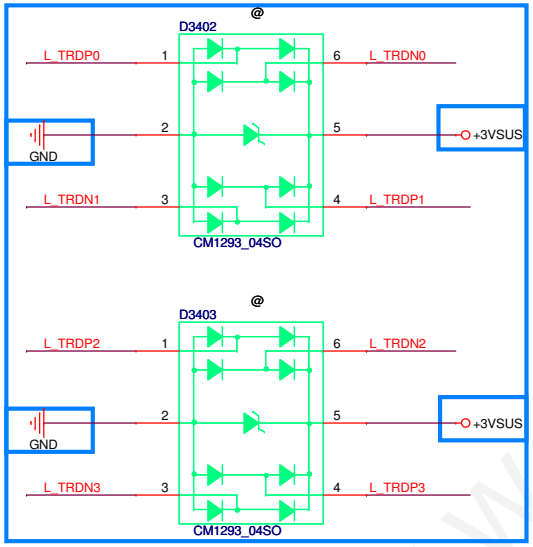




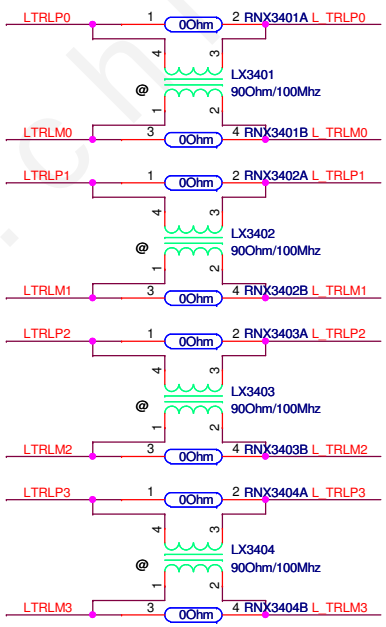


R1.0 1105 Delete D3401

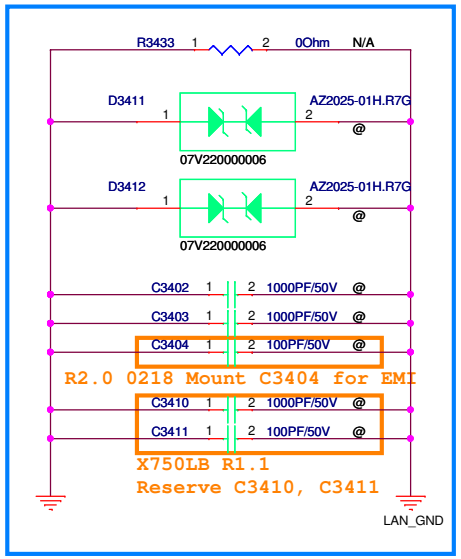
R1.0 1026 EMI
建議將TVS (D3402, D3403) 放置在一出transformer往chip方向的位置,
change net define



R1.0 1031 change power rail of D3402, D3403
R1.0 1105 change LAN_GND to GND



R1.0 1018 EMI



PEGATRON	Title : RJ45/ RJ11	
BG1-HW RD Center-HW RD Div.2-HW RD Dept2-HB Sec.2	Engineer: Johnson Huang	
Size: Custom	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 34 of 100	

www.chinafix.com

www.chinafix.com

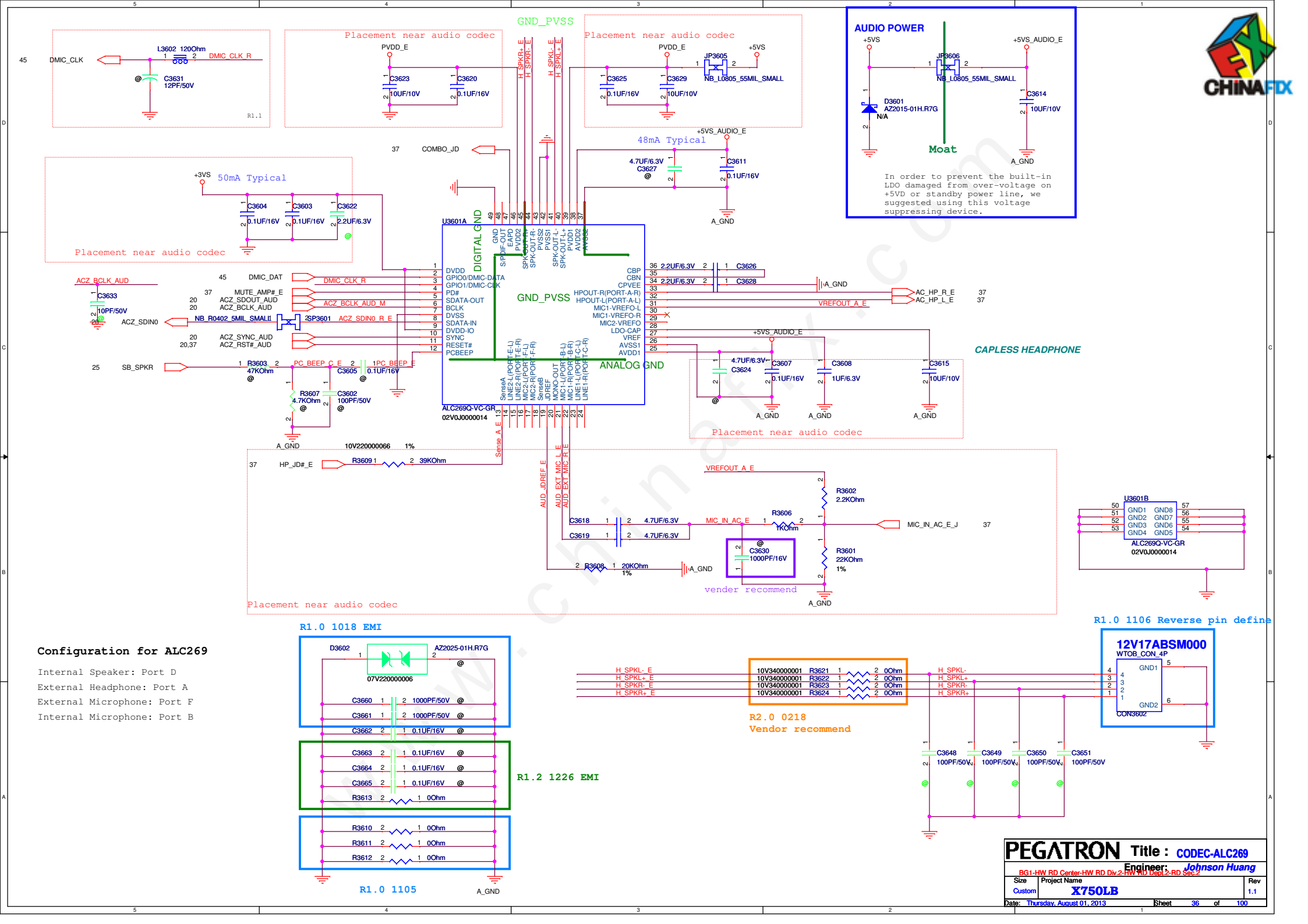
PEGATRON Title :

Engineer: Johnson Huang

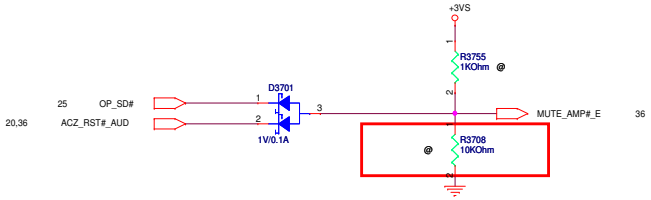
BG1-HW RD Center-HW RD Div.2-HW RD Sec.2

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 35 of 100


AUDIO POWER
+5VS
+5VS_AUDIO_E
JP3606
NB_L0805_55MIL_SMALL
D3601
AZ2015-01H.R7G
N/A
C3614
10UF/10V
Moat
A_GND
In order to prevent the built-in LDO damaged from over-voltage on +5VD or standby power line, we suggested using this voltage suppressing device.
GND_PVSS
Placement near audio codec
PVDD_E
C3623
10UF/10V
C3620
0.1UF/16V
C3625
C3629
JP3605
48mA Typical
C3627
4.7UF/6.3V
C3611
0.1UF/16V
+3VS
50mA Typical
C3604
C3603
C3622
2.2UF/6.3V
U3601A
DIGITAL GND
ANALOG GND
ALC269Q-VC-GR
02V0J0000014
DVDD
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BCLK
DVSS
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
CBP
CBN
CPVEE
HPOUT-R(PORT-A-R)
HPOUT-L(PORT-A-L)
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDD1
C3626
C3628
AC_HP_R_E
AC_HP_L_E
VREFOUT_A_E
CAPLESS HEADPHONE
C3633
10PF/50V
ACZ_BCLK_AUD
ACZ_SDIN0
DMIC_DAT
DMIC_CLK_R
MUTE_AMP#_E
ACZ_SDOUT_AUD
ACZ_BCLK_AUD
ACZ_BCLK_AUD_M
NB_R0402_5MIL_SMALL
SP3601
ACZ_SDIN0_R_E
ACZ_SYNC_AUD
ACZ_RST#_AUD
SB_SPKR
R3603
47KOhm
PC_BEEP_C_E
C3605
0.1UF/16V
PC_BEEP_E
R3607
4.7KOhm
C3602
100PF/50V
C3624
4.7UF/6.3V
C3607
0.1UF/16V
C3608
1UF/6.3V
C3615
10UF/10V
HP_JD#_E
R3609
39KOhm
10V220000066
1%
AUD_JDREF_E
AUD_EXT_MIC_L_E
AUD_EXT_MIC_R_E
C3618
C3619
4.7UF/6.3V
MIC_IN_AC_E
R3606
1KOhm
R3602
2.2KOhm
R3601
22KOhm
1%
R3608
20KOhm
C3630
1000PF/16V
vender recommend
MIC_IN_AC_E_J
U3601B
ALC269Q-VC-GR
02V0J0000014
R1.0 1106 Reverse pin define
12V17ABSM000
WTOB_CON_4P
CON3602
R1.0 1018 EMI
D3602
AZ2025-01H.R7G
07V220000006
C3660
C3661
1000PF/50V
C3662
C3663
C3664
C3665
0.1UF/16V
R3613
R3610
R3611
R3612
0Ohm
R1.2 1226 EMI
R1.0 1105
H_SPKL-_E
H_SPKL+_E
H_SPKR-_E
H_SPKR+_E
10V340000001
R3621
R3622
R3623
R3624
H_SPKL-
H_SPKL+
H_SPKR-
H_SPKR+
R2.0 0218
Vendor recommend
C3648
C3649
C3650
C3651
100PF/50V
Configuration for ALC269
Internal Speaker: Port D
External Headphone: Port A
External Microphone: Port F
Internal Microphone: Port B
PEGATRON
Title : CODEC-ALC269
Engineer: Johnson Huang
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2
Size
Custom
Project Name
X750LB
Rev
1.1
Date: Thursday, August 01, 2013
Sheet 36 of 100

AMP De-Pop Control circuit

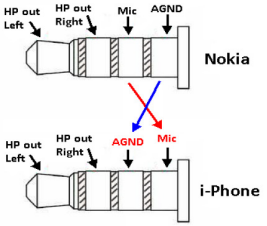


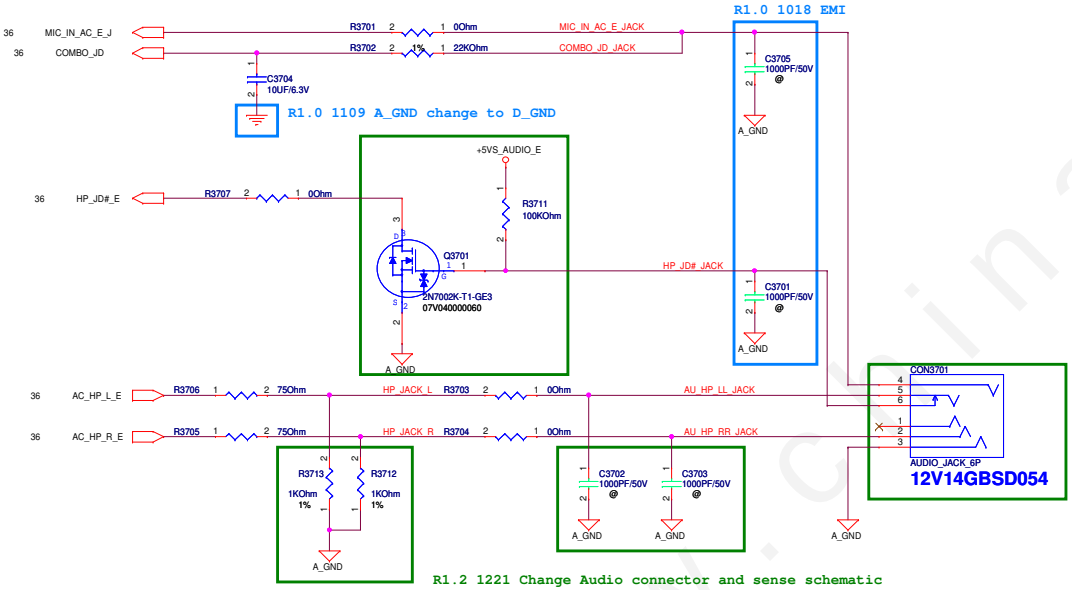
unmount R3708 for speaker issue

Moat D_GND

A_GND

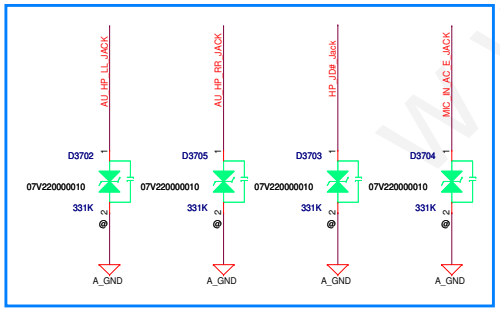
HP/MIC Combo JACK (for i-Phone only)





R1.2 1221 Change Audio connector and sense schematic
Add Q3701, R3711, R3712, R3713

R1.0 1030 EMI



PEGATRON	Title : AUDIO Jack	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2	Engineer: Johnson Huang	
Size: C	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 37 of 100	

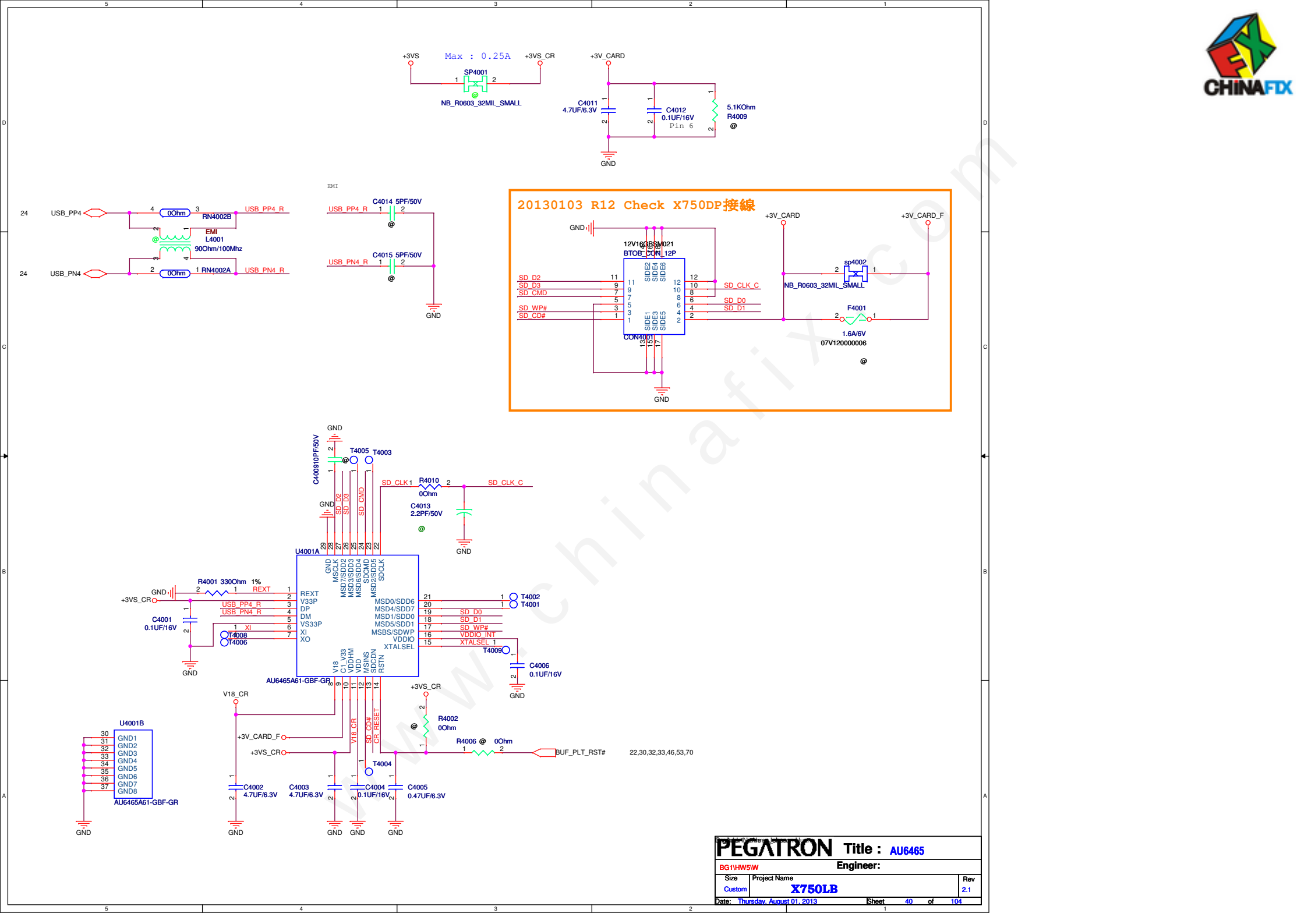
www.chinafix.com

www.chinafix.com

Title	<Title>	
Size: A	Document Number: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 38 of 100	

www.chinafix.com

Title	<Title>	
Size: A	Document Number: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 39 of 100	



PEGATRON

Title : AU6465

BG1\HW5\W

Engineer:

Size	Project Name	Rev
Custom	X750LB	2.1

Date: Thursday, August 01, 2013 Sheet 40 of 104

www.chinafix.com

www.chinafix.com

PEGATRON	Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 41 of 100	

www.chinafix.com

PEGATRON

Title :

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2

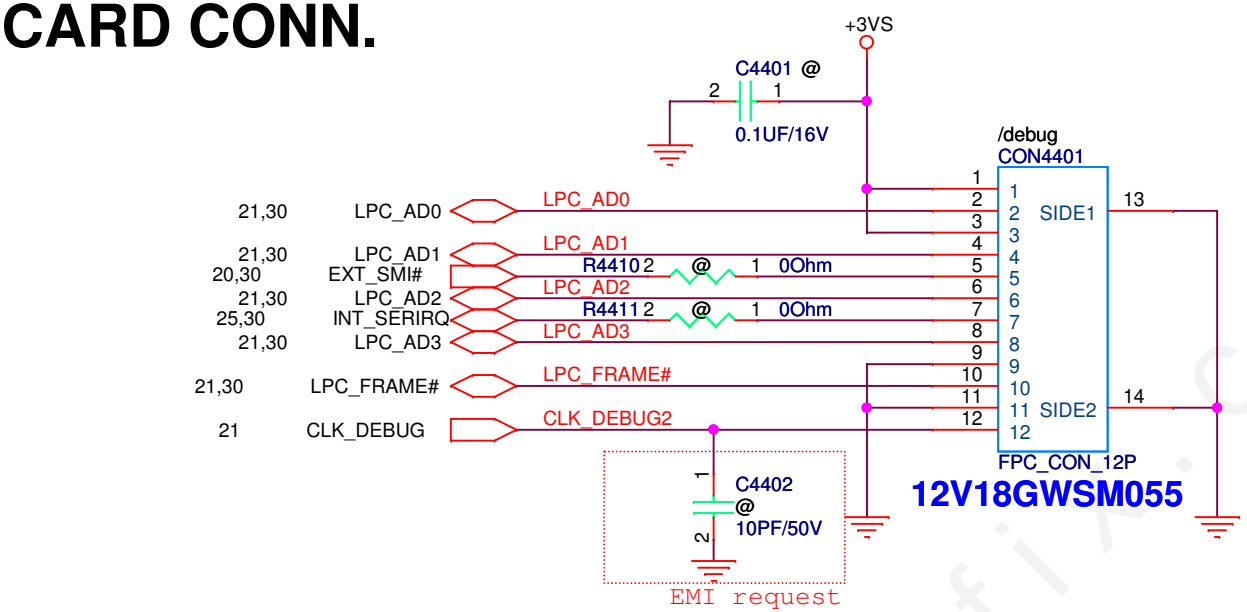
Size	Project Name	Rev
A	X750LB	1.1

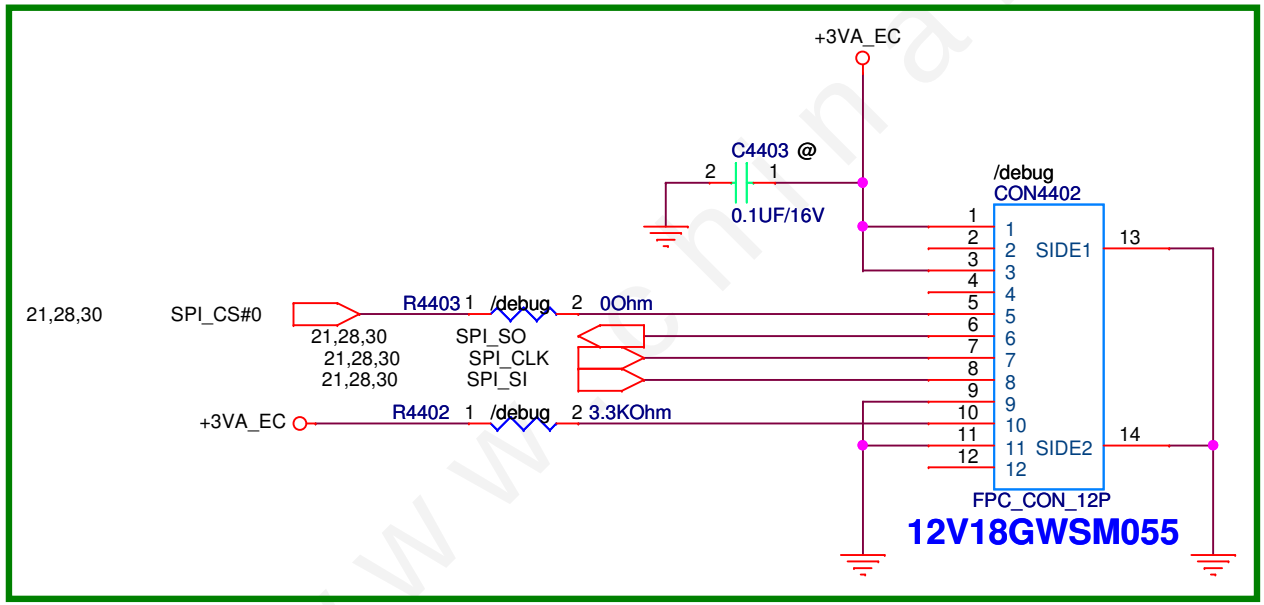
Date: Thursday, August 01, 2013 Sheet 42 of 100

www.chinafix.com

PEGATRON	Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 43 of 100	

DEBUG CARD CONN.

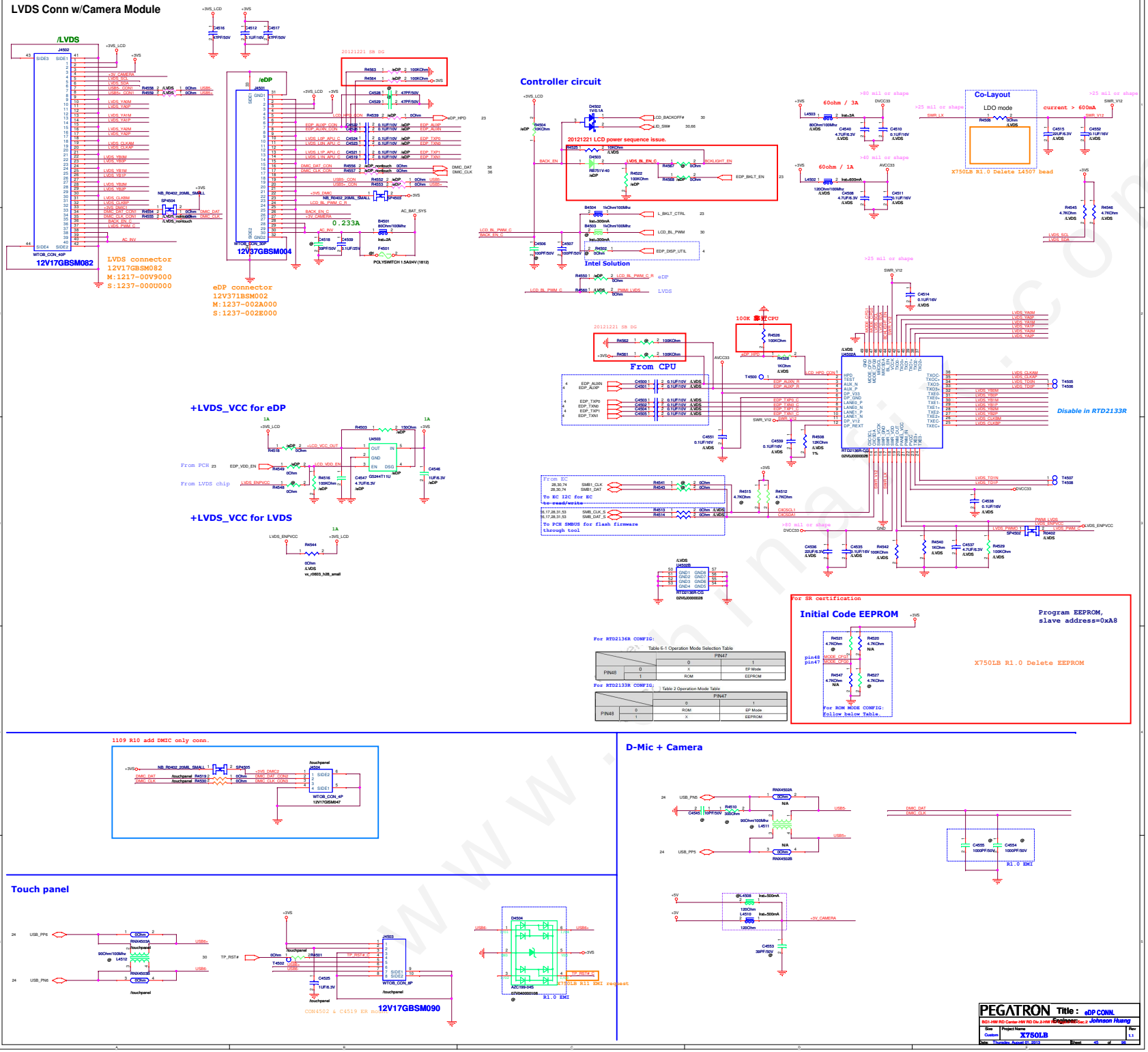




R1.2 1220 Change the connection of CON4402
from U2802(BIOS) to U2801(ME)

PEGATRON	Title : DEBUG CONN.	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 44 of 100	

LVDS Conn w/Camera Module



www.chinafix.com

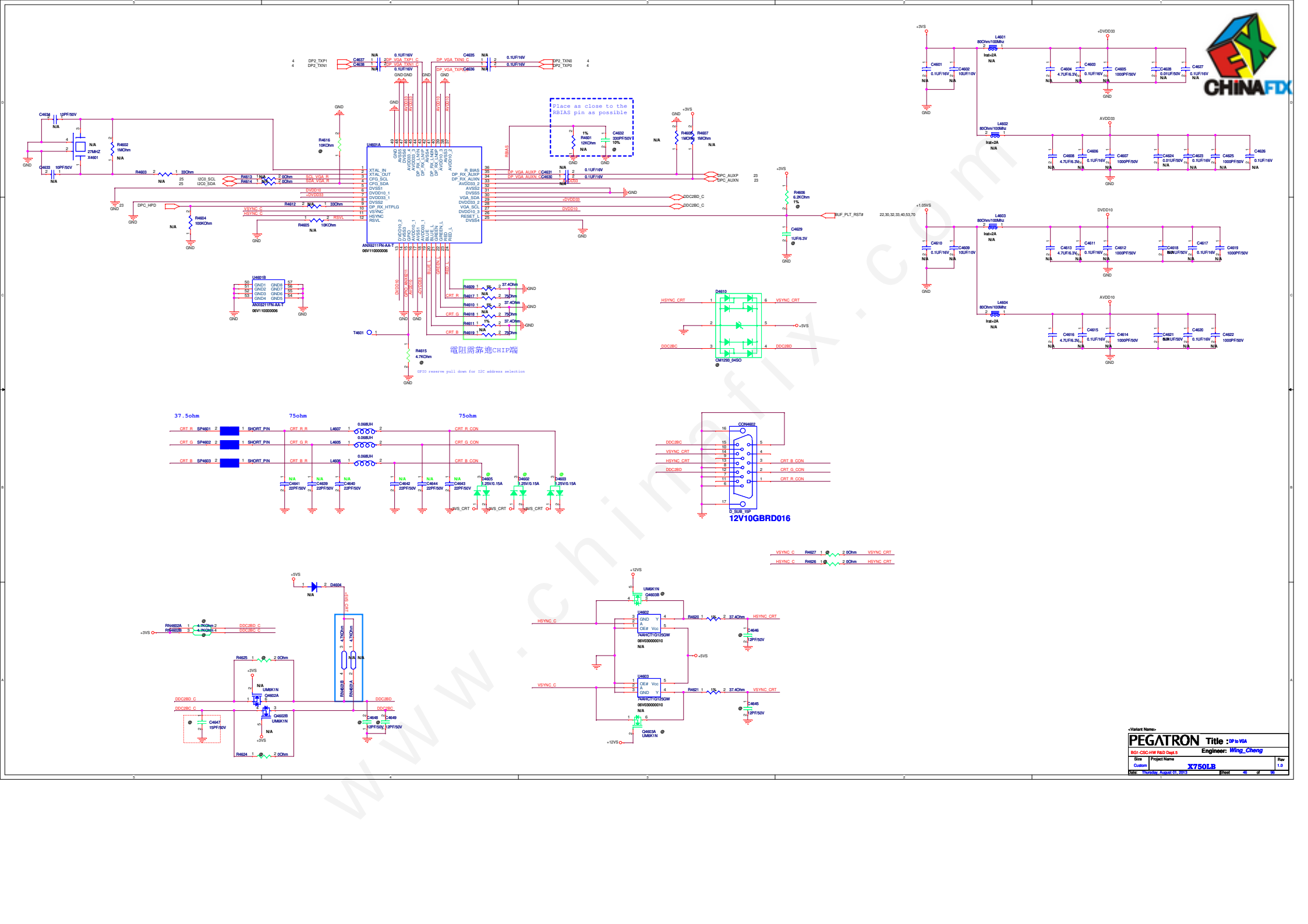
PEGATRON Title : eDP CONN.

Engineer: Johnson Huang

Project Name: X750LB

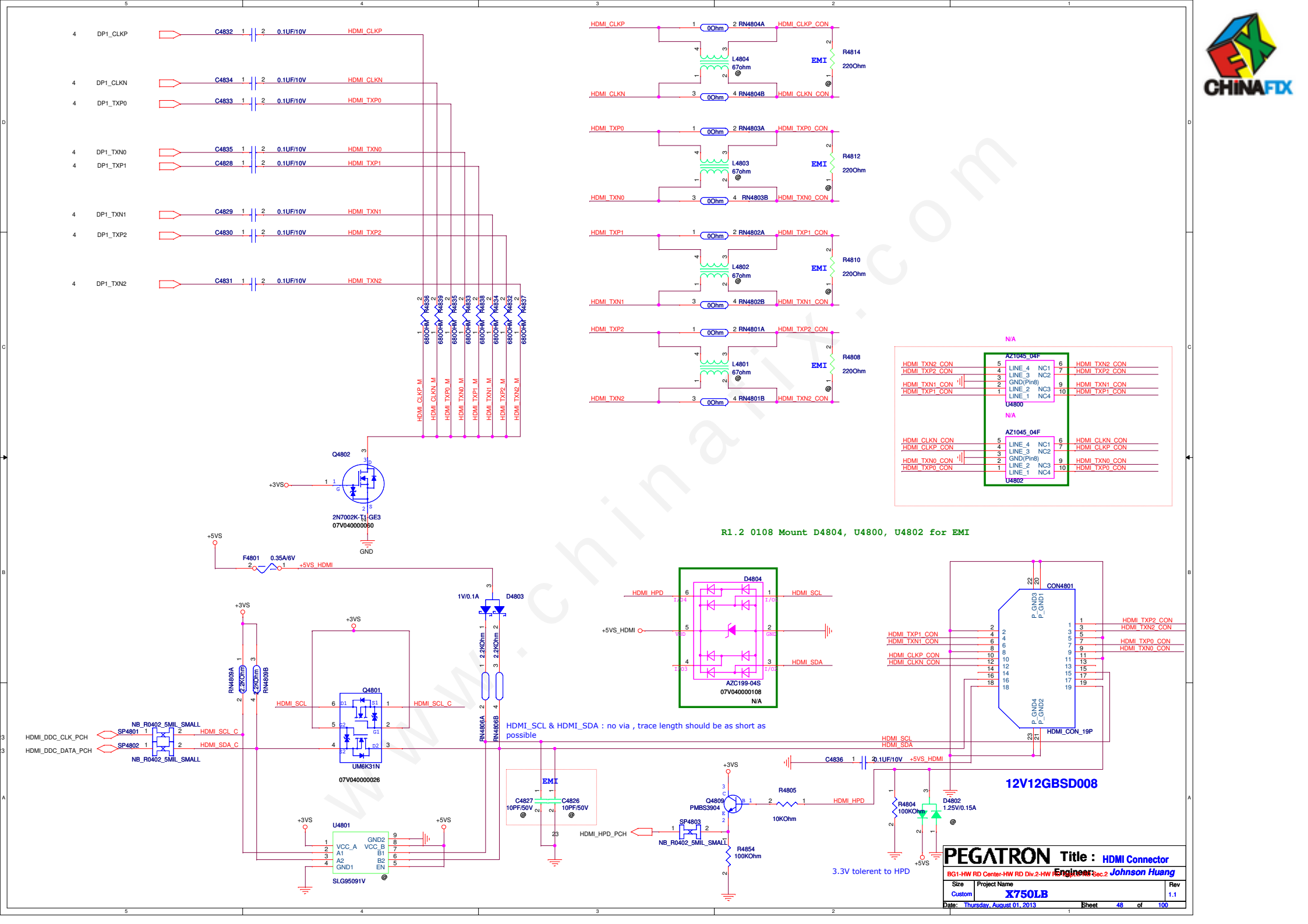
Rev: 1.1

Date: Thursday, August 01, 2013 Sheet 45 of 55


Place as close to the RBIAS pin as possible
電阻需靠進CHIP端
GPIO reserve pull down for I2C address selection
37.5ohm
75ohm
75ohm
12V10GBRD016
X750LB
PEGATRON
Title : DP to VGA
Engineer: Wing_Cheng
Thursday, August 01, 2013

www.chinafix.com

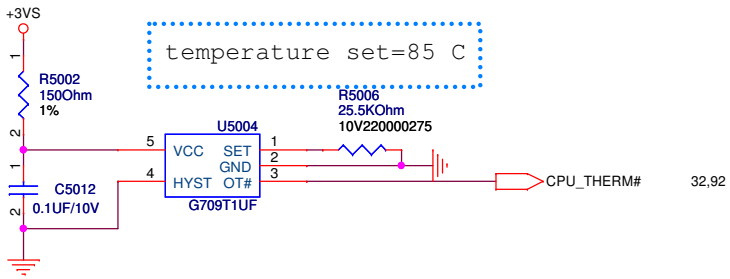
PEGATRON	Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 47 of 100	


DP1_CLKP
DP1_CLKN
DP1_TXP0
DP1_TXN0
DP1_TXP1
DP1_TXN1
DP1_TXP2
DP1_TXN2
C4832 0.1UF/10V HDMI_CLKP
C4834 0.1UF/10V HDMI_CLKN
C4833 0.1UF/10V HDMI_TXP0
C4835 0.1UF/10V HDMI_TXN0
C4828 0.1UF/10V HDMI_TXP1
C4829 0.1UF/10V HDMI_TXN1
C4830 0.1UF/10V HDMI_TXP2
C4831 0.1UF/10V HDMI_TXN2
680OHM R4836
680OHM R4839
680OHM R4835
680OHM R4833
680OHM R4838
680OHM R4834
680OHM R4832
680OHM R4837
HDMI_CLKP_M
HDMI_CLKN_M
HDMI_TXP0_M
HDMI_TXN0_M
HDMI_TXP1_M
HDMI_TXN1_M
HDMI_TXP2_M
HDMI_TXN2_M
HDMI_CLKP 0Ohm RN4804A HDMI_CLKP_CON
HDMI_CLKN 0Ohm RN4804B HDMI_CLKN_CON
L4804 67ohm @
R4814 220Ohm
HDMI_TXP0 0Ohm RN4803A HDMI_TXP0_CON
HDMI_TXN0 0Ohm RN4803B HDMI_TXN0_CON
L4803 67ohm @
R4812 220Ohm
HDMI_TXP1 0Ohm RN4802A HDMI_TXP1_CON
HDMI_TXN1 0Ohm RN4802B HDMI_TXN1_CON
L4802 67ohm @
R4810 220Ohm
HDMI_TXP2 0Ohm RN4801A HDMI_TXP2_CON
HDMI_TXN2 0Ohm RN4801B HDMI_TXN2_CON
L4801 67ohm @
R4808 220Ohm
EMI
N/A
AZ1045_04F
U4800
U4802
HDMI_TXN2_CON
HDMI_TXP2_CON
HDMI_TXN1_CON
HDMI_TXP1_CON
HDMI_CLKN_CON
HDMI_CLKP_CON
HDMI_TXN0_CON
HDMI_TXP0_CON
Q4802
2N7002K-T1-GE3
07V040000060
+3VS
GND
+5VS
F4801 0.35A/6V
+5VS_HDMI
1V/0.1A
D4803
D4804
AZC199-04S
07V040000108
HDMI_HPD
HDMI_SCL
HDMI_SDA
RN4809A 2.2KOhm
RN4809B 2.2KOhm
RN4806A 2.2KOhm
RN4806B 2.2KOhm
Q4801
UM6K31N
07V040000026
HDMI_SCL_C
HDMI_SDA_C
NB_R0402_5MIL_SMALL
SP4801
SP4802
HDMI_DDC_CLK_PCH
HDMI_DDC_DATA_PCH
HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible
U4801
SLG95091V
EMI
C4827 10PF/50V @
C4826 10PF/50V @
C4836 0.1UF/10V +5VS_HDMI
Q4809 PMBS3904
R4805 10KOhm
R4804 100KOhm
D4802 1.25V/0.15A @
SP4803
R4854 100KOhm
HDMI_HPD_PCH
3.3V tolerent to HPD
CON4801
HDMI_CON_19P
P_GND3
P_GND1
P_GND4
P_GND2
HDMI_TXP2_CON
HDMI_TXN2_CON
HDMI_TXP0_CON
HDMI_TXN0_CON
HDMI_TXP1_CON
HDMI_TXN1_CON
HDMI_CLKP_CON
HDMI_CLKN_CON
R1.2 0108 Mount D4804, U4800, U4802 for EMI
12V12GBSD008
PEGATRON
Title : HDMI Connector
Engineer: Johnson Huang
Size Custom
Project Name X750LB
Rev 1.1
Date: Thursday, August 01, 2013
Sheet 48 of 100

www.chinafix.com

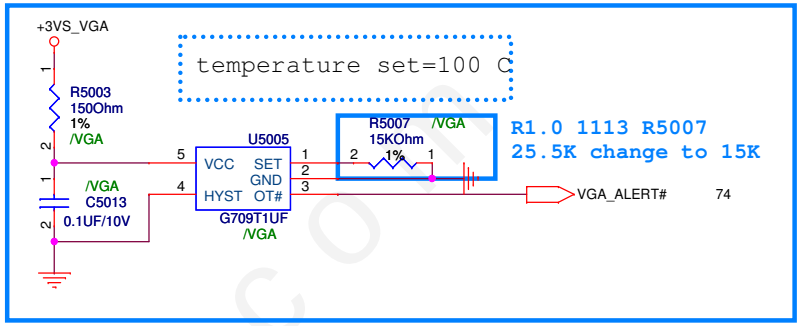
PEGATRON	Title : HDMI CEC	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.-HW Sec.2	Engineer: Johnson Huang	
Size: Custom	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 49 of 100	

CPU Thermal Sensor

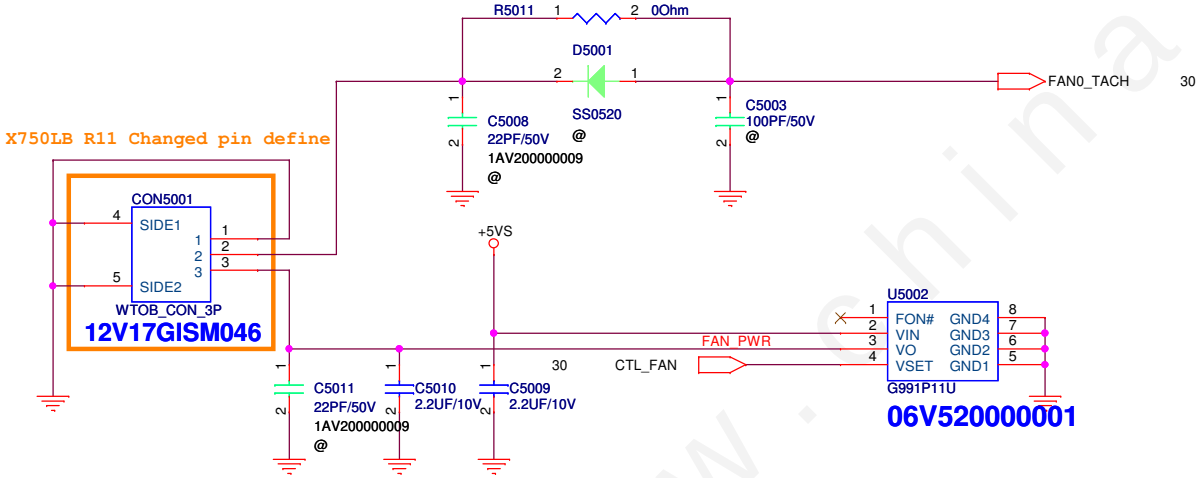


GPU Thermal Sensor

R1.0 1031 Thermal Request(ABBA DFA)



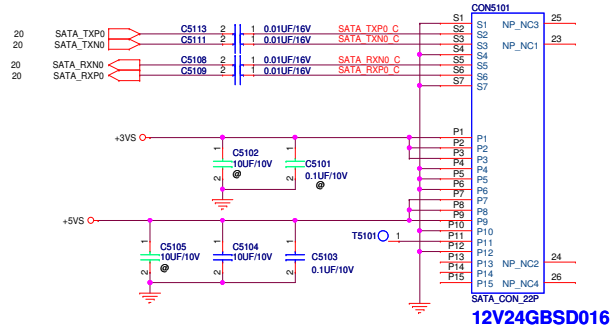
FAN



PEGATRON	Title : FAN / Thermal Sensor	
	Engineer: Johnson Huang	
Size: Custom	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 50 of 100	

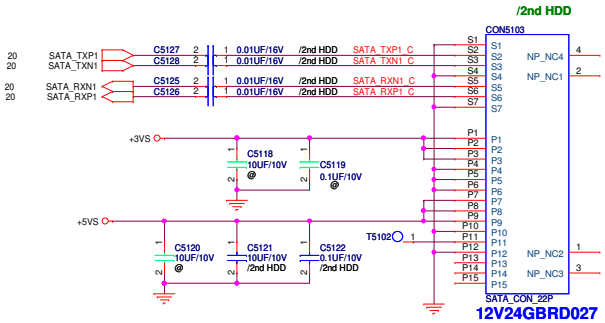
www.chinafix.com

HDD



12V24GBSD016

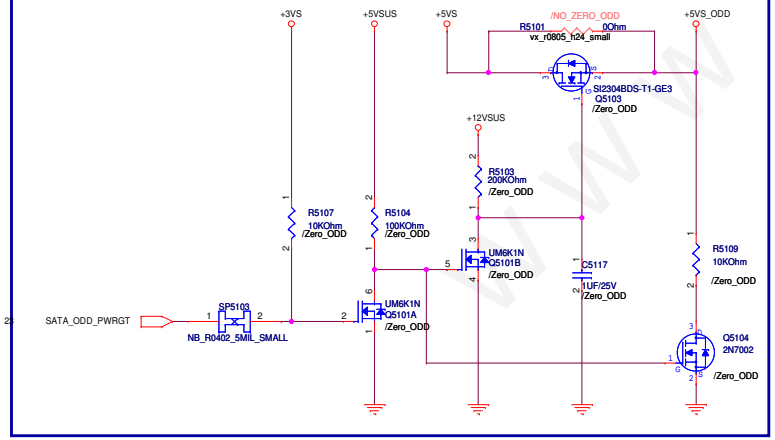
2nd HDD



12V24GBRD027

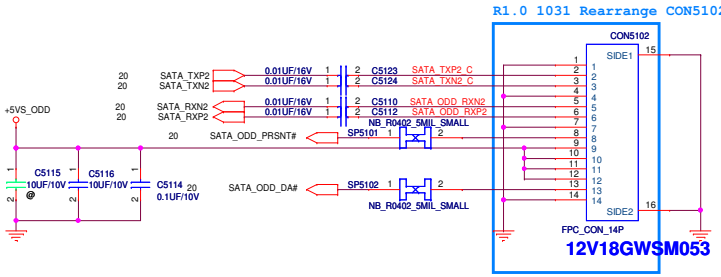
ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



ODD

R1.0 1031 Rearrange CON5102 pin define

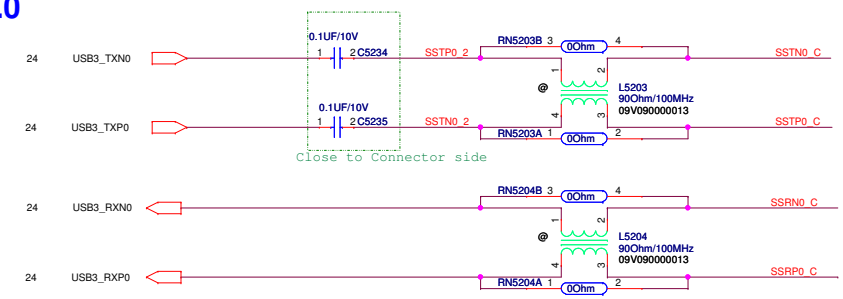


12V18GWSM053

PEGATRON	Title : HDD & ODD	
BG1-HW RD Center-HW RD Div.2-HW RD Sec.2	Engineer: Johnson Huang	
Size: C	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 51 of 100	

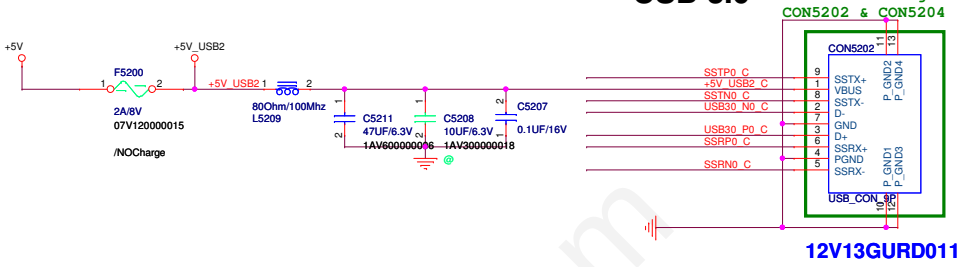
www.chinafix.com

Left USB3.0



USB 3.0

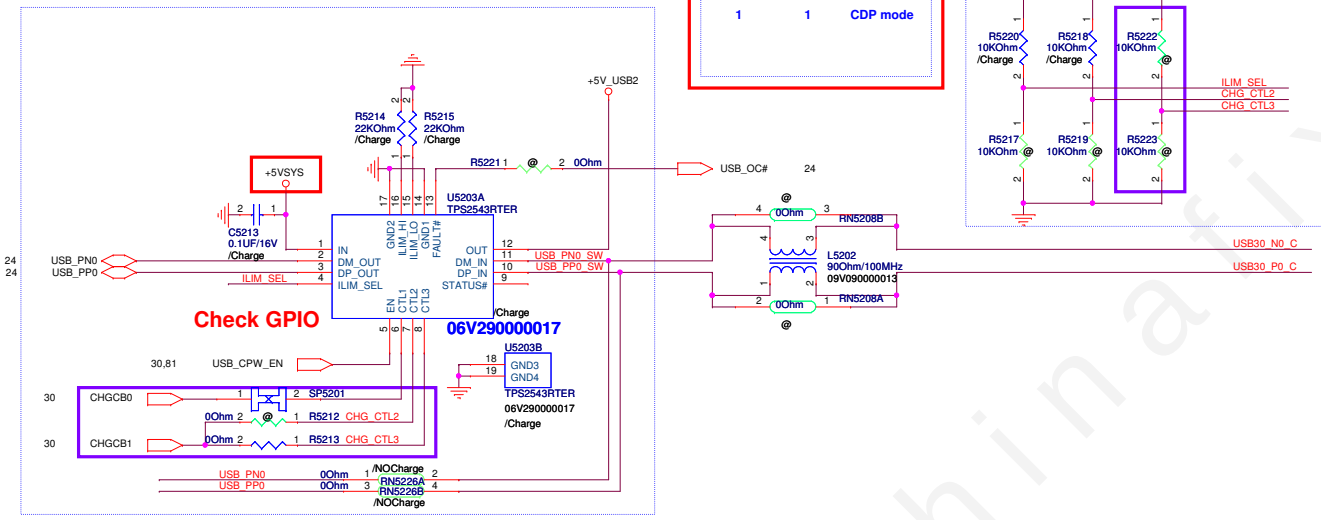
R1.2 1221 Change connector
CON5202 & CON5204



12V13GURD011

Sleep & Charge (only 1 pcs)

TPS2543



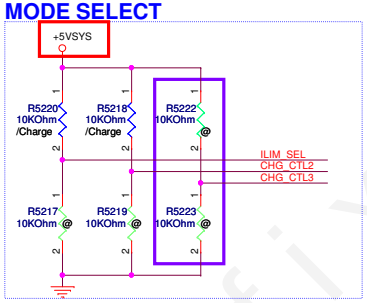
X750LB R11 modify for USB Charger issue

Check truth table

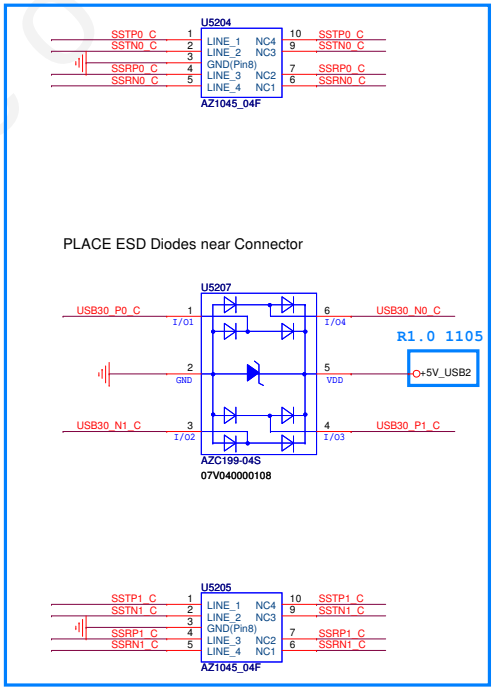
* ILIM_SEL = H, CHG_CTL3 = H

CTL1	CTL3	FUNCTION
0	1	Auto mode
1	1	CDP mode

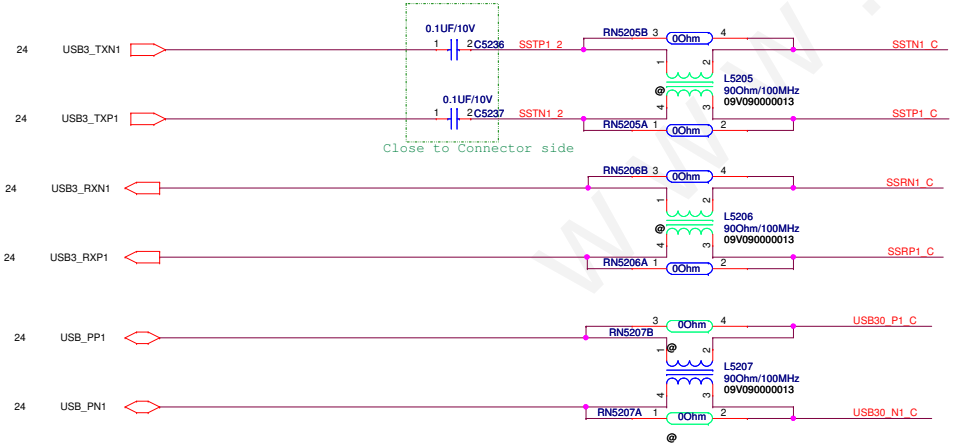
MODE SELECT

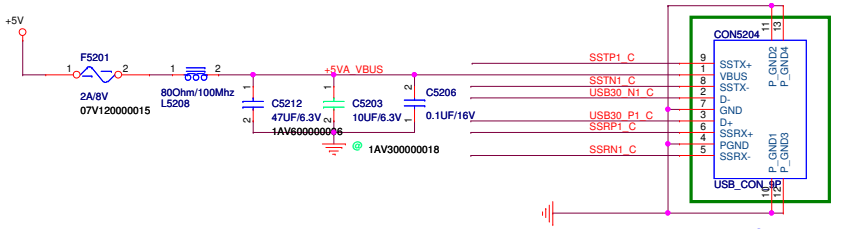


R1.0 1018 EMI



USB 3.0



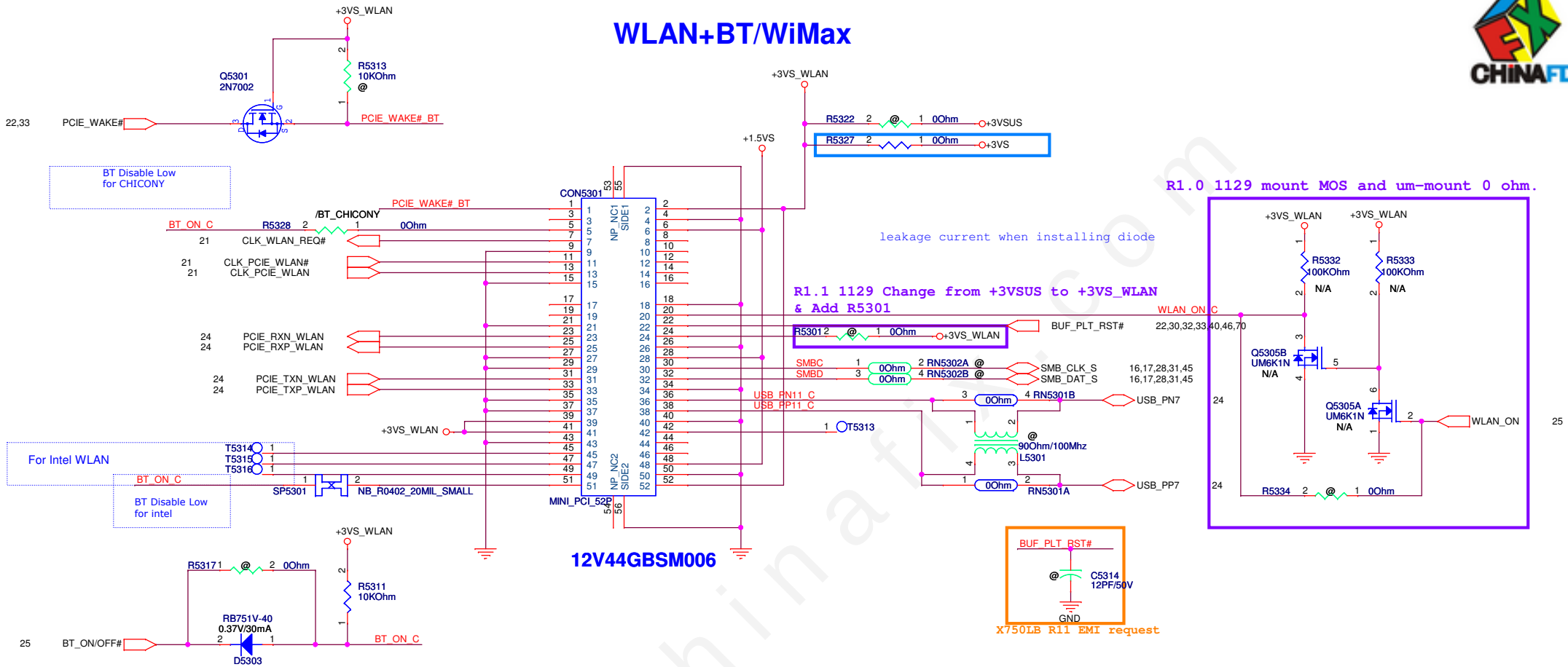


12V13GURD011

PEGATRON	Title : USB PORTS	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.-HW Sec.2	Engineer: Johnson Huang	
Size: Custom	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 52 of 100	

www.chinafix.com

WLAN+BT/WiMax

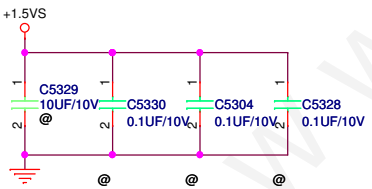


H = 6.5 mm

WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

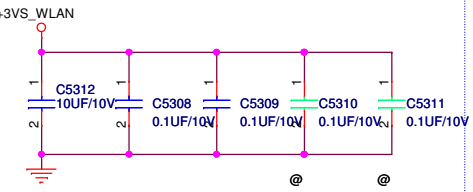
Place 10UF near +1.5VS source side.



WLAN +3VS bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VS_WLAN source side.



PEGATRON	Title : MINICARD WLAN	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.1 RD Sect.2	Engineer: Johnson Huang	
Size: B	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 53 of 100	

www.chinafix.com

www.chinafix.com

PEGATRON Title : Mini Card

BG1-HW RD Center-HW RD Div.2-HW RD Dept.-HW RD Sec.2 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 54 of 100

Camera

+3VS	+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+3V	+3V	22,45,57,91
+5V	+5V	45,52,57,66,91

www.chinafix.com

PEGATRON Title : *******

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2

Size	Project Name	Rev
A	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 55 of 100

+5VSUS	+5VSUS	22,26,4,51,81,83
+3VA	+3VA	20,26,30,57,81,88,91,93
+3VS	+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+5VA	+5VA	81,91
+5V	+5V	45,52,57,66,91
+5VS	+5VS	20,30,36,46,48,50,51,57,66,80,87,91

Touch Pad Button

Power LED
LED5608

Power switch
SW5604

Power Button

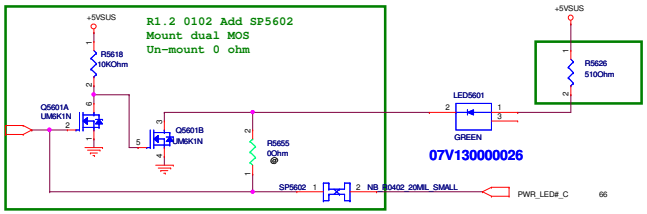
Wireless Button

LED Placement
Left-->Right

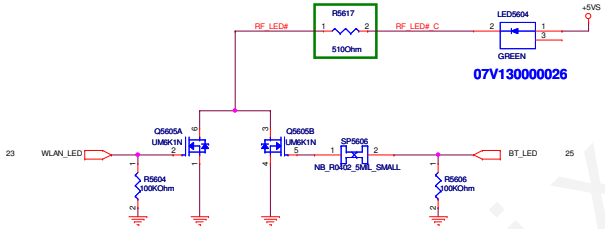
Power LED LED5601 | Charger LED LED5602 | HDD LED LED5603 | RF LED LED5604 | Num Lock LED LED5605 | Caps Lock LED LED5606

Power LED

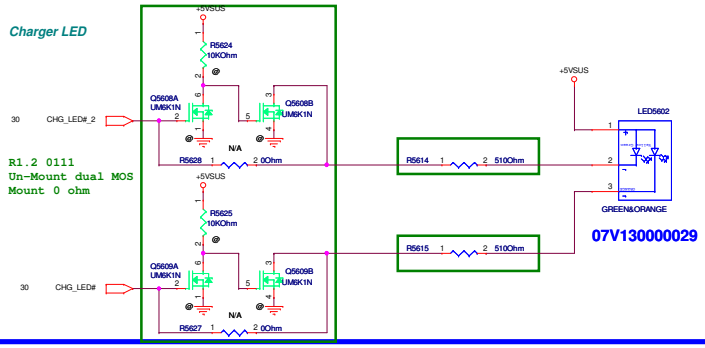
R1.2 0108 Change all LED resistance = 510 ohm



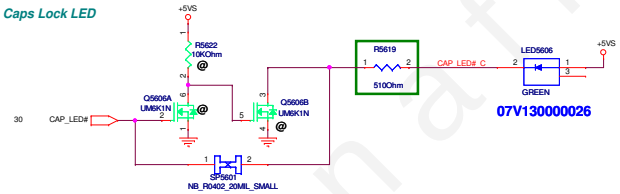
RF LED



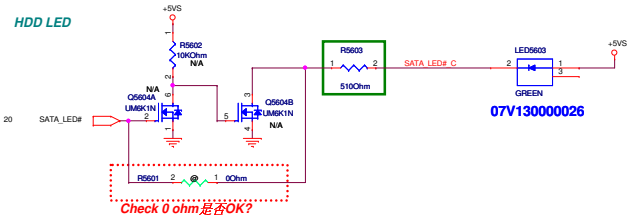
Charger LED



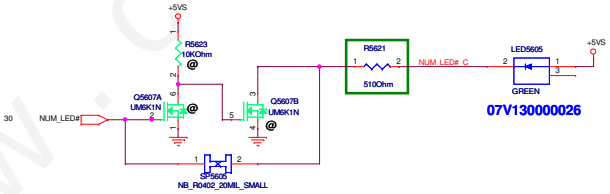
Caps Lock LED



HDD LED



Num Lock LED



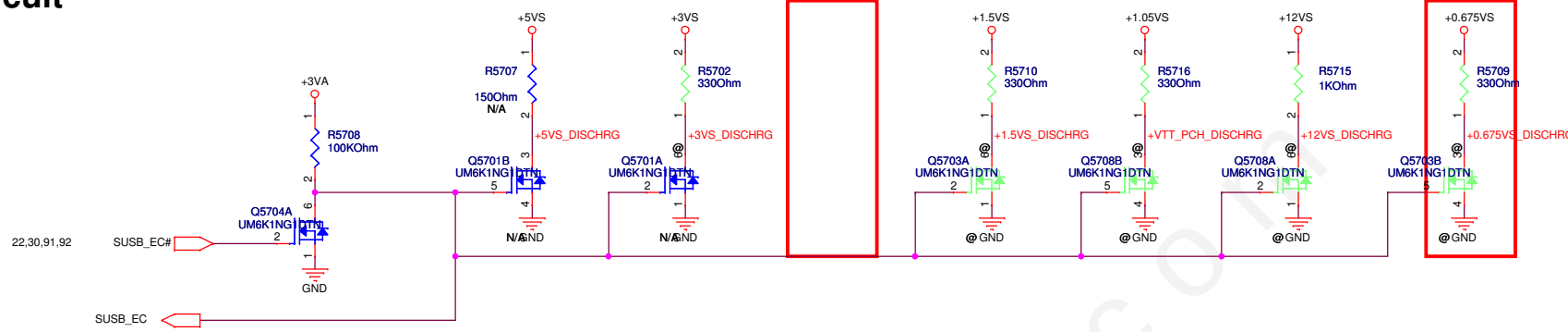
PEGATRON	Title : LED_Indicator		
BG1-HW RD Center-HW RD Div.2-HW RD Sec.2	Engineer: Johnson Huang		
Size: Custom	Project Name: X750LB		Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 56 of 100		

www.chinafix.com

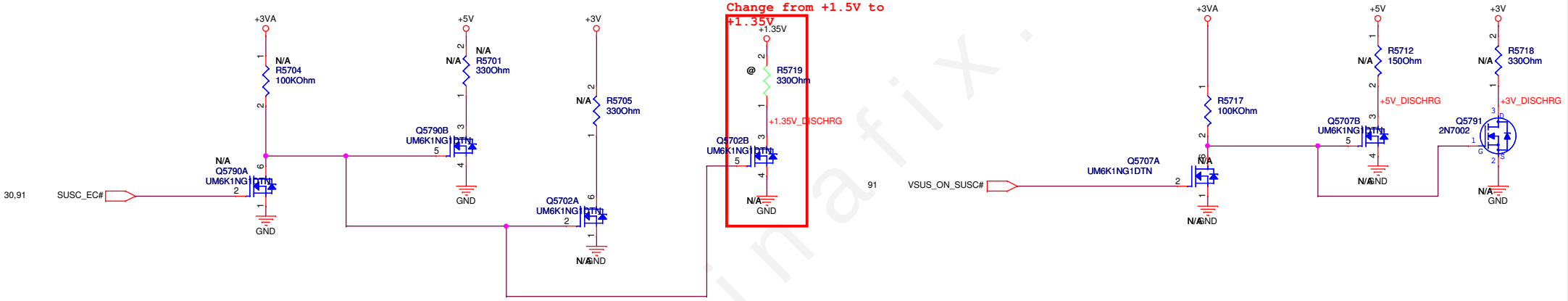
Discharge Circuit

1020 R10 Remove +1.8VS

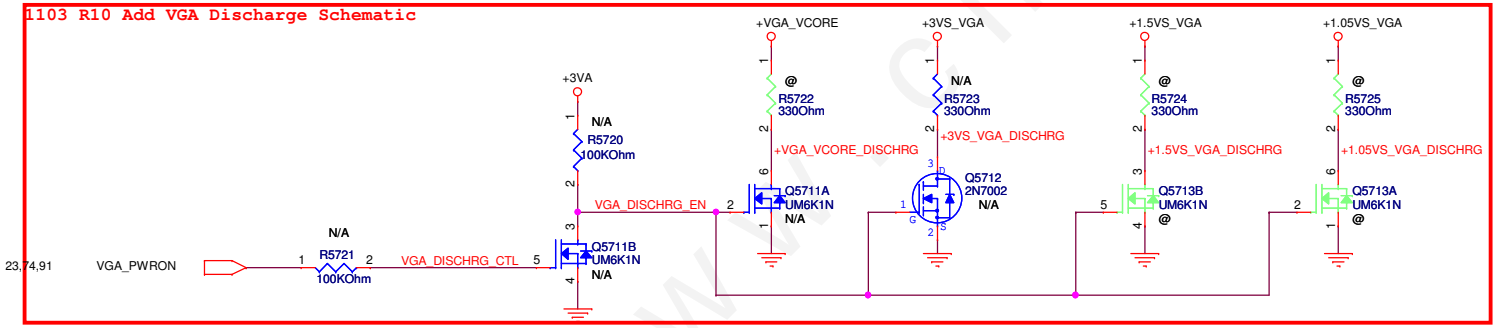
1020 R10
Change from +0.75VS to +0.675VS



1020 R10
Change from +1.5V to +1.35V



1103 R10 Add VGA Discharge Schematic



PEGATRON	Title : DISCHARGE CKT	
BG1_BU2	Engineer: Shiro_Lin	
Size: Custom	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 57 of 96	

www.chinafix.com

www.chinafix.com

PEGATRON Title : ASM1042

BG1-HW RD Center-HW RD Div.2-HW RD Dept.-HW RD Sec.2 Engineer: Johnson Huang

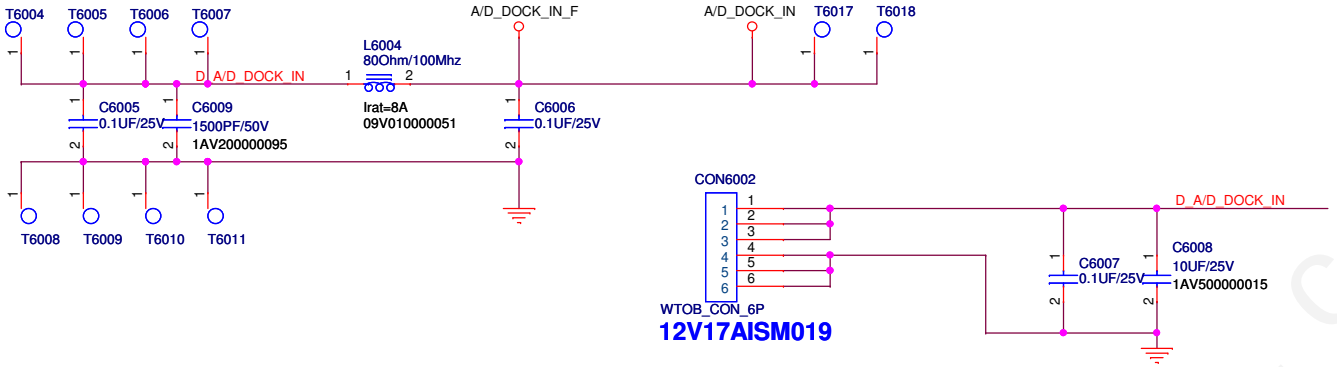
Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 58 of 100

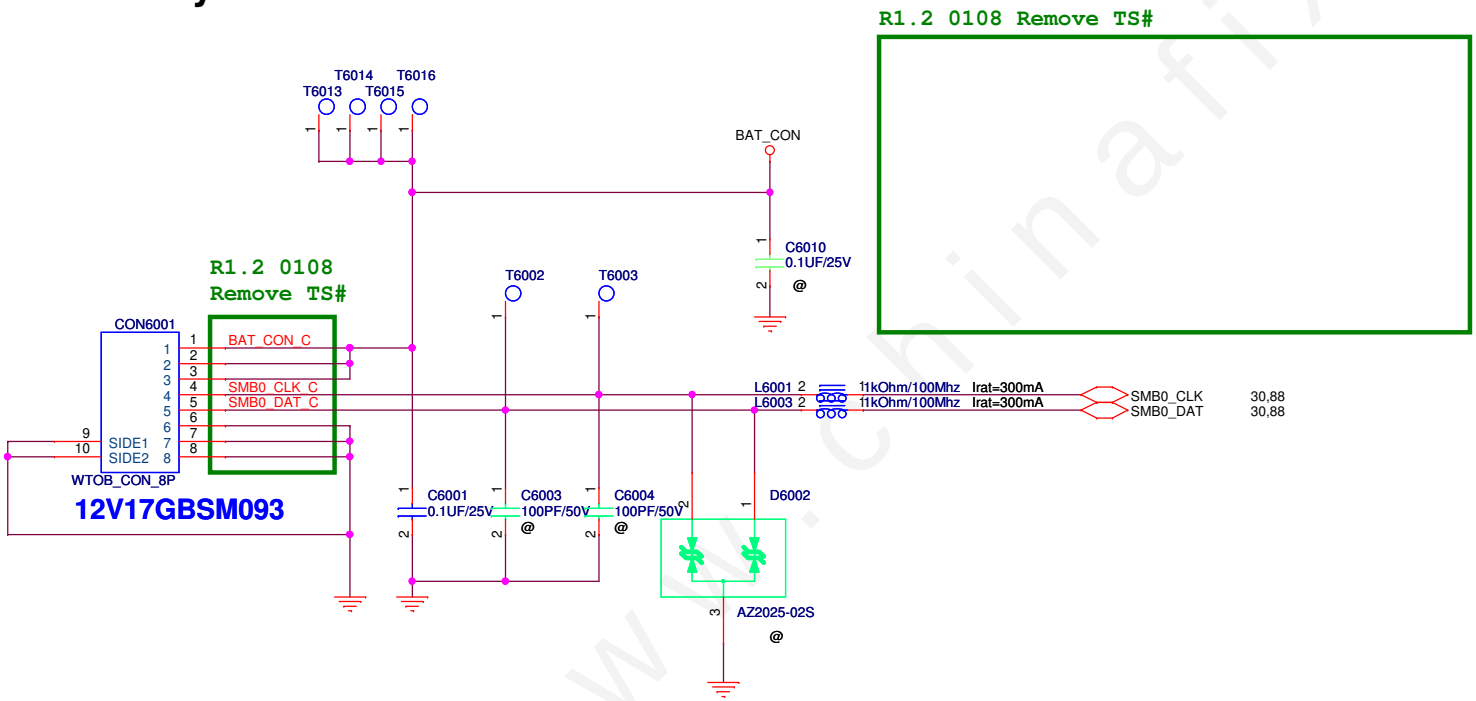
www.chinafix.com

PEGATRON	Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 59 of 100	

DC IN



Battery Connector



www.chinafix.com

PEGATRON	Title : DC IN/ Battery Connector	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2	Engineer: Johnson Huang	
Size: Custom	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 60 of 100	

www.chinafix.com

PEGATRON	Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 61 of 100	

www.chinafix.com

PEGATRON

Title :

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2

Size	Project Name	Rev
A	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 62 of 100

www.chinafix.com

PEGATRON	Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2	Engineer: Johnson Huang	
Size: A	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 63 of 100	

www.chinafix.com

PEGATRON

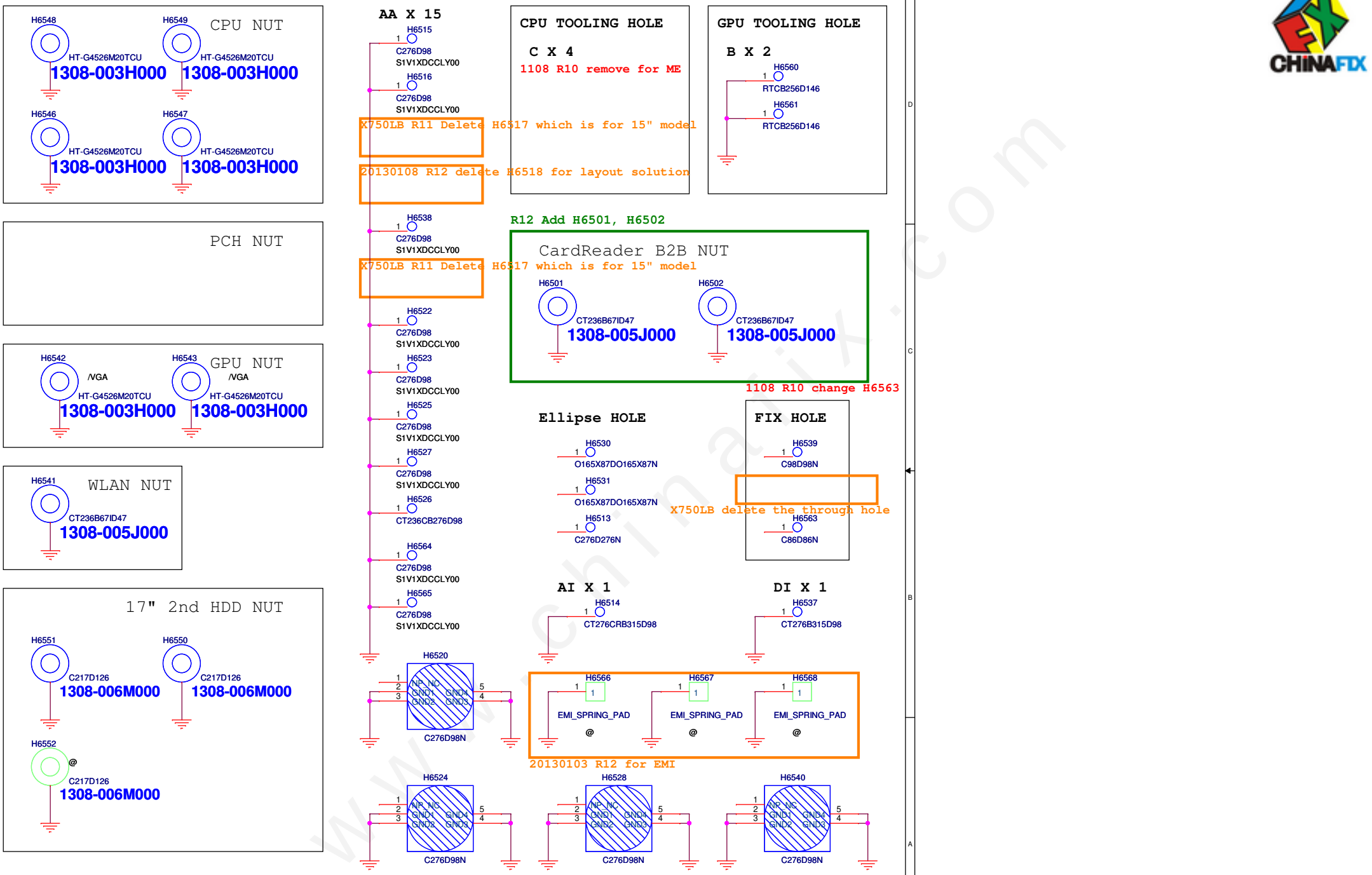
Title :

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-RD Sec.2

Size	Project Name	Rev
A	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 64 of 100



PEGATRON Title : ME_CONN,Skew Hole

Engineer: Louis Chang

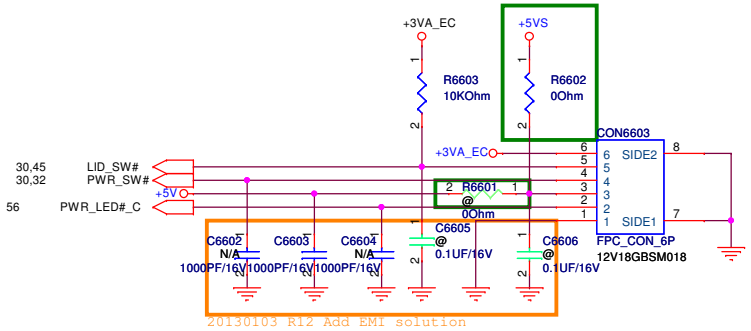
Size	Project Name	Rev
Custom	Q500A	2.0

Date: Thursday, August 01, 2013 Sheet 65 of 98

www.chinafix.com

PWR BRD

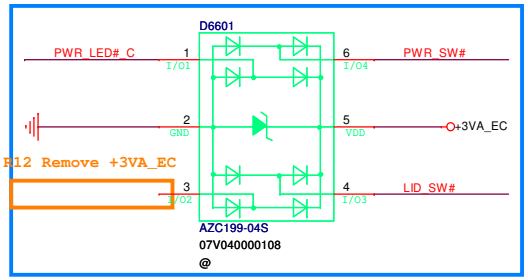
20130218 R20 Add for S3 Power LED on Power Button off



20130103 R12 Add EMI solution

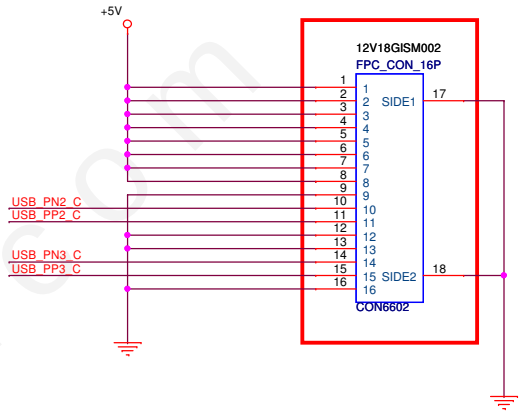
R1.0 0928 Remove debounce(add debounce at PWR BD side)

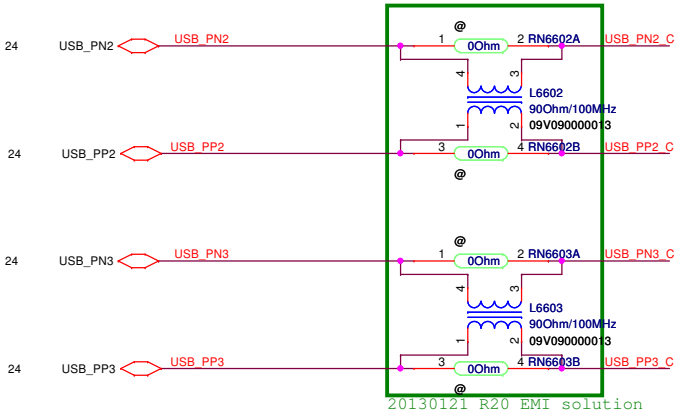
R1.0 1018 EMI



20130103 R12 Remove +3VA_EC

+5V	+5V	45,52,57,91
+3VS	+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+5VSUS	+5VSUS	22,26,4,51,56,81,83
+3VA_EC	+3VA_EC	28,30,32,44





20130121 R20 EMI solution

www.chinafix.com

PEGATRON Title : PWR BRD/IO BRD

BG1_BU2 Engineer: Shiro_Lin

Size	Project Name	Rev
Custom	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 66 of 100

www.chinafix.com

PEGATRON Title :

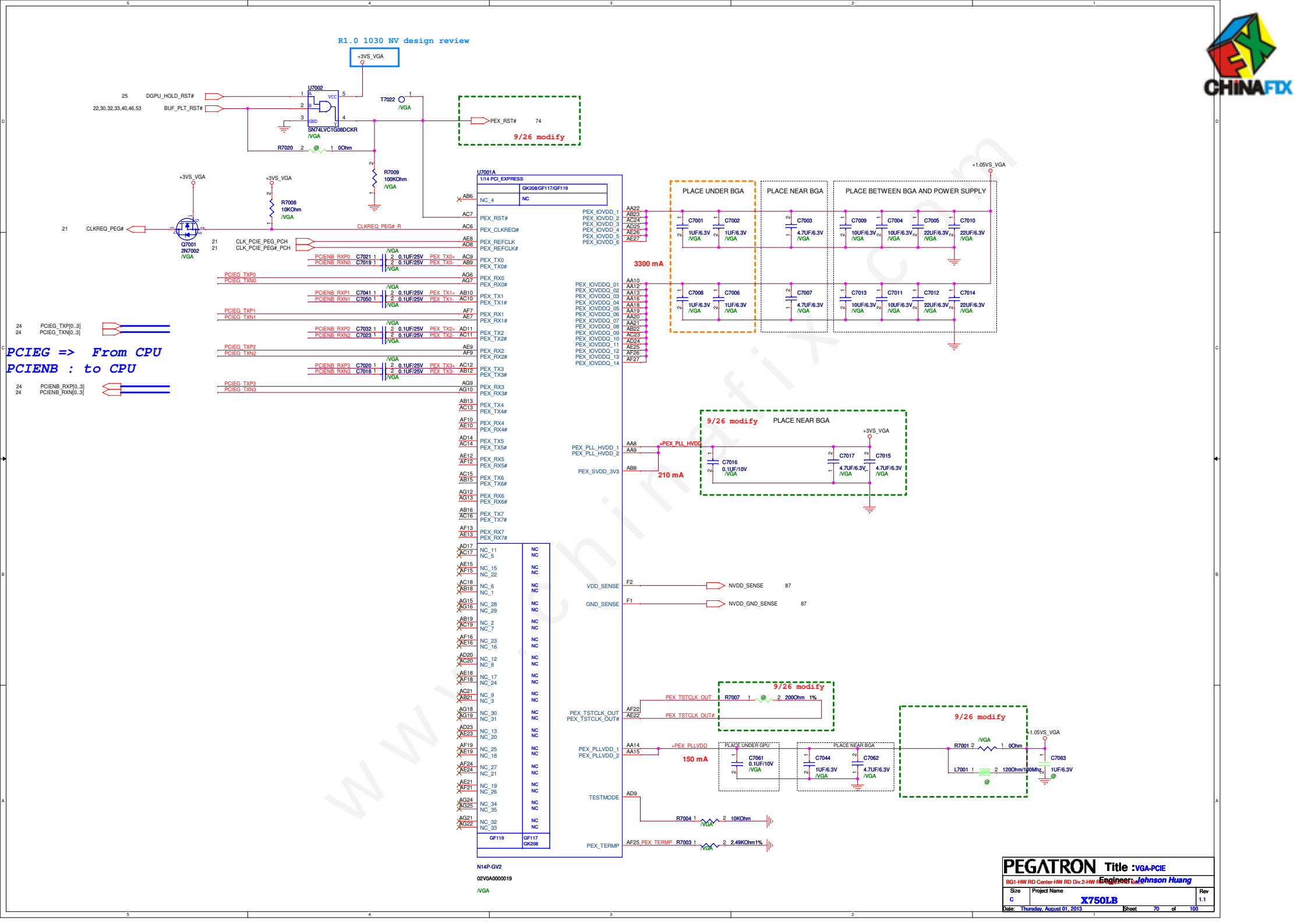
BG1-HW RD Center-HW RD Div.2-HW RD Dept.-HB SA...

Engineer: Johnson Huang

Size	Project Name	Rev
Custom	Comal	1.1

Date: Thursday, August 01, 2013 Sheet 67 of 100

R1.0 1030 NV design review

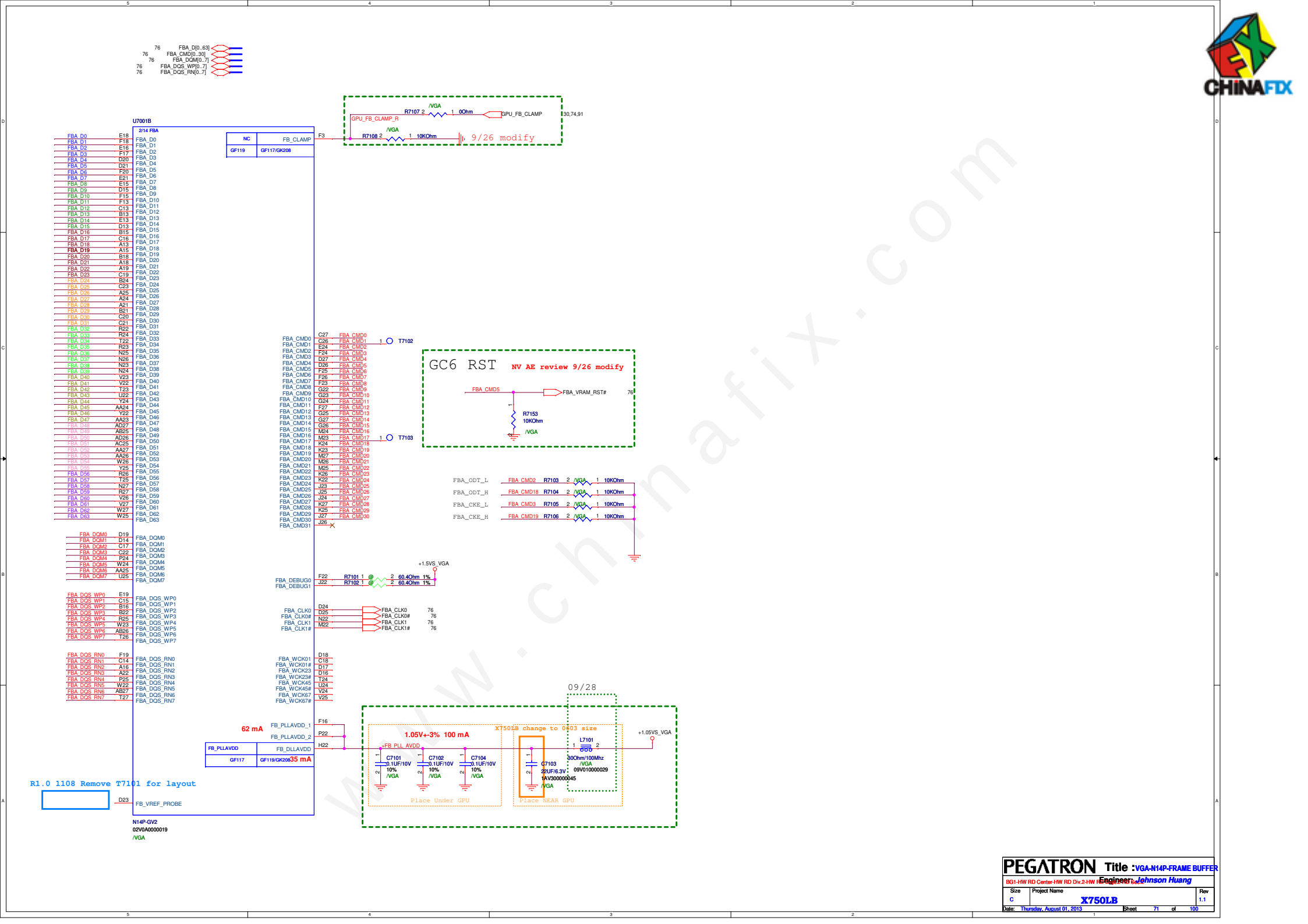


PEGATRON Title : VGA-PCIE

Engineer: Johnson Huang

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 70 of 100



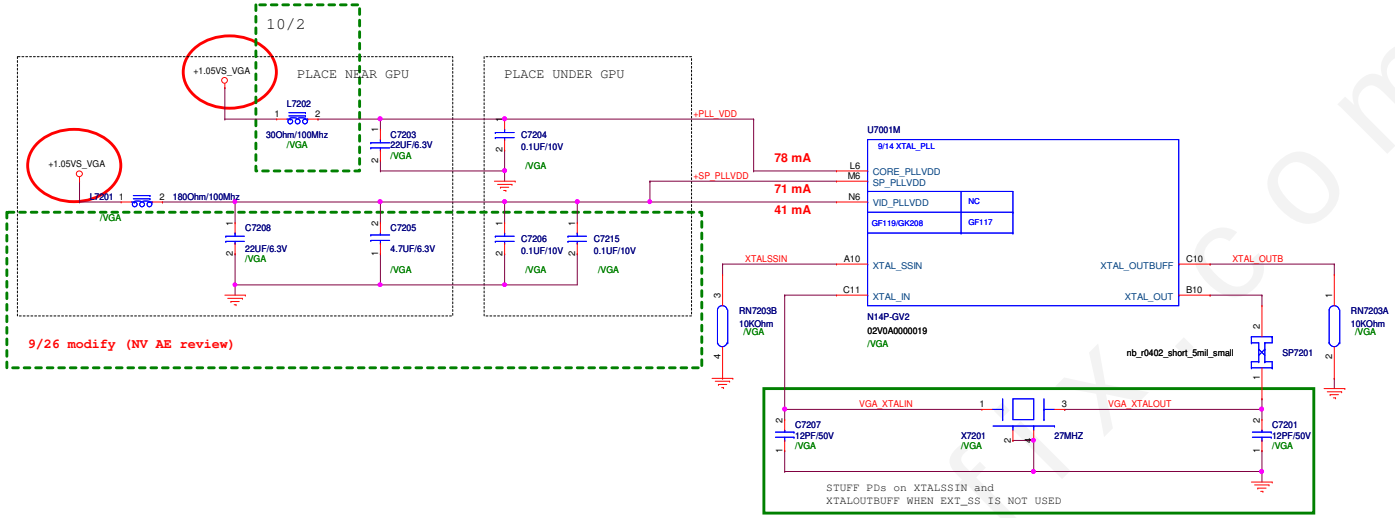
www.chinafix.com

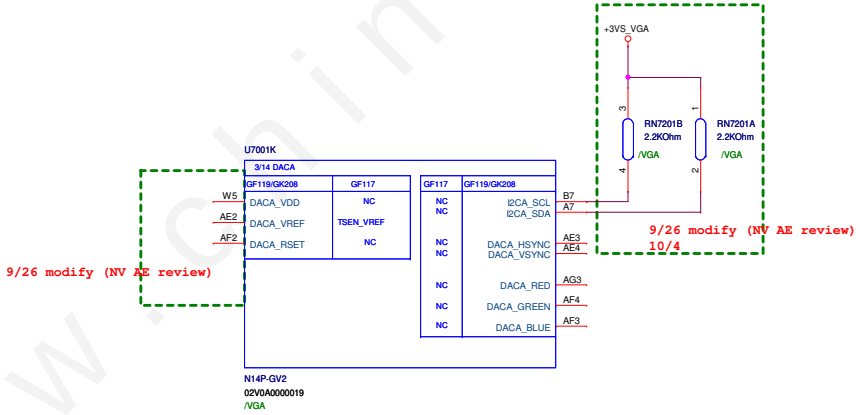
PEGATRON Title : VGA-N14P-FRAME BUFFER

Engineer: Johnson Huang

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 71 of 100





www.chinafix.com

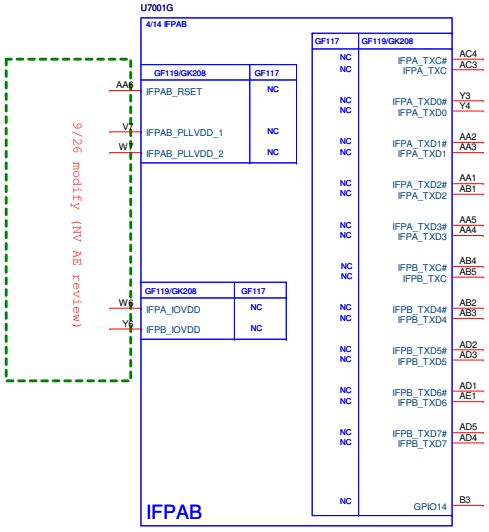
PEGATRON Title : VGA_RGB,XTAL

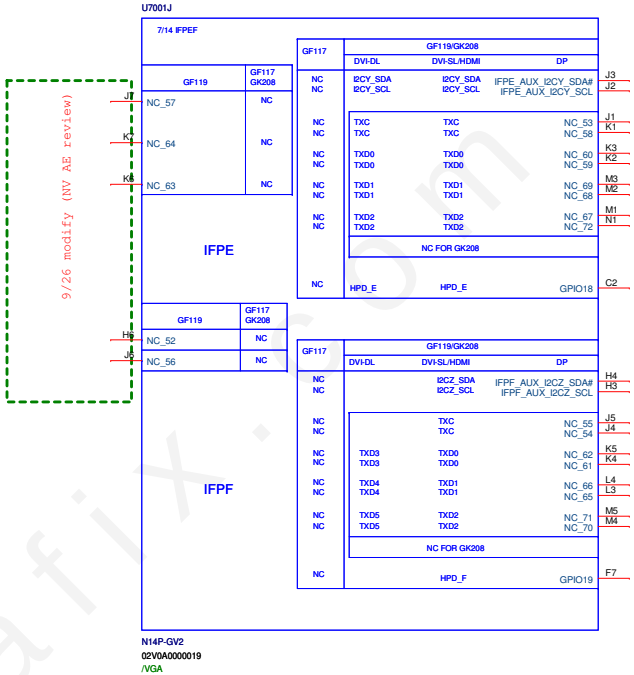
Engineer: Johnson Huang

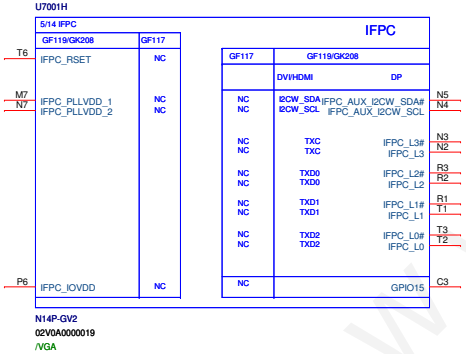
Size	Project Name	Rev
C	X750LB	1.1

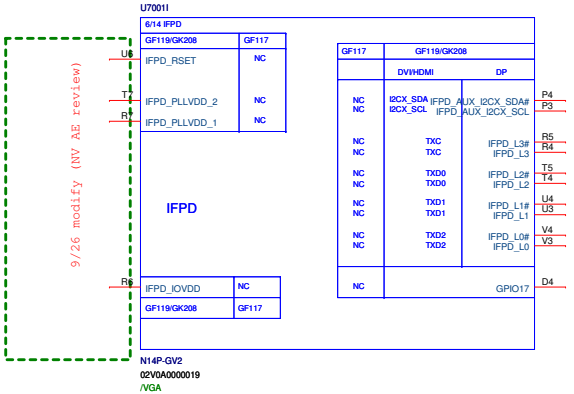
Date: Thursday, August 01, 2013 Sheet 72 of 100

LVDS









www.chinafix.com

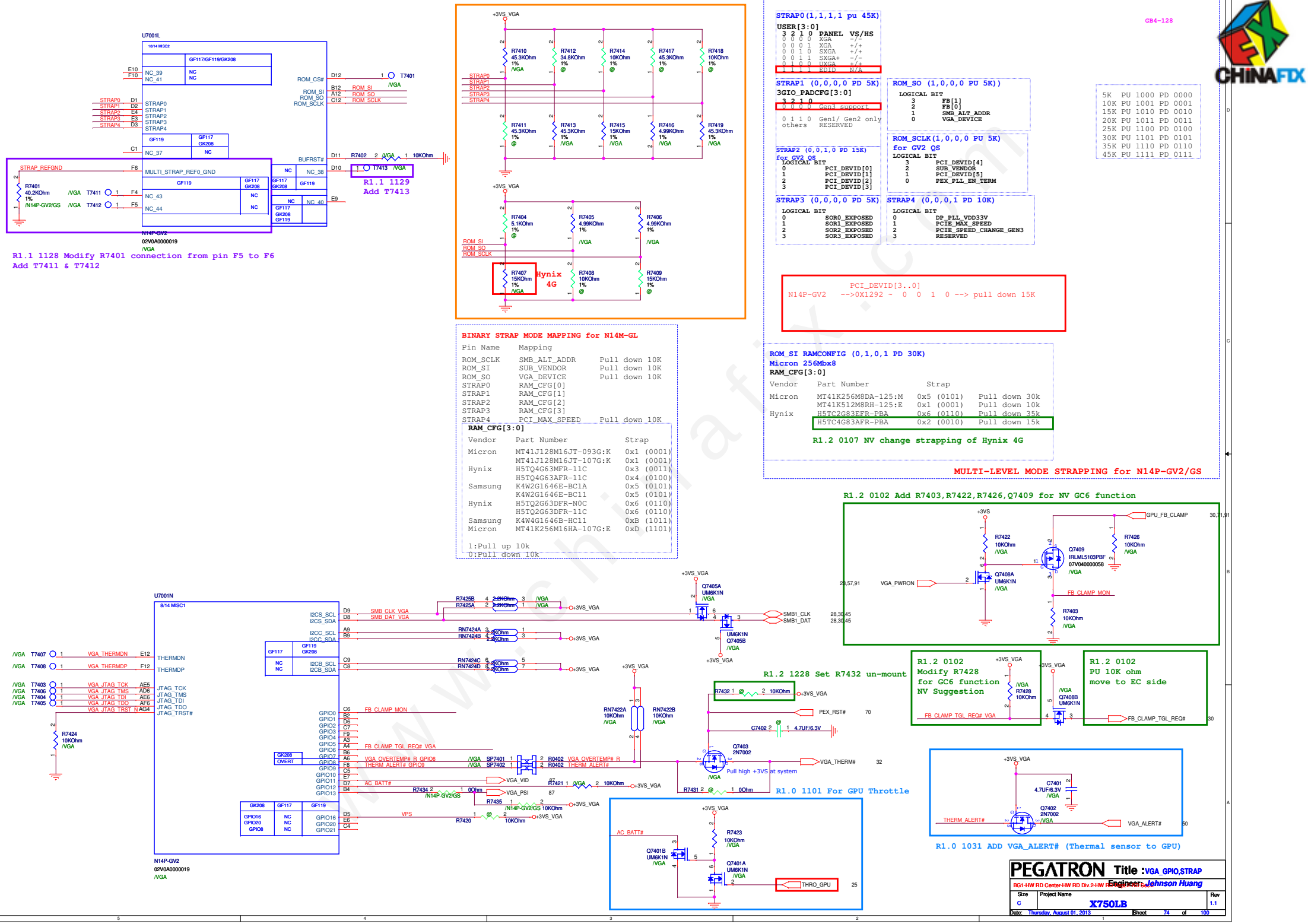
PEGATRON Title : VGA_LVDS_HDMI

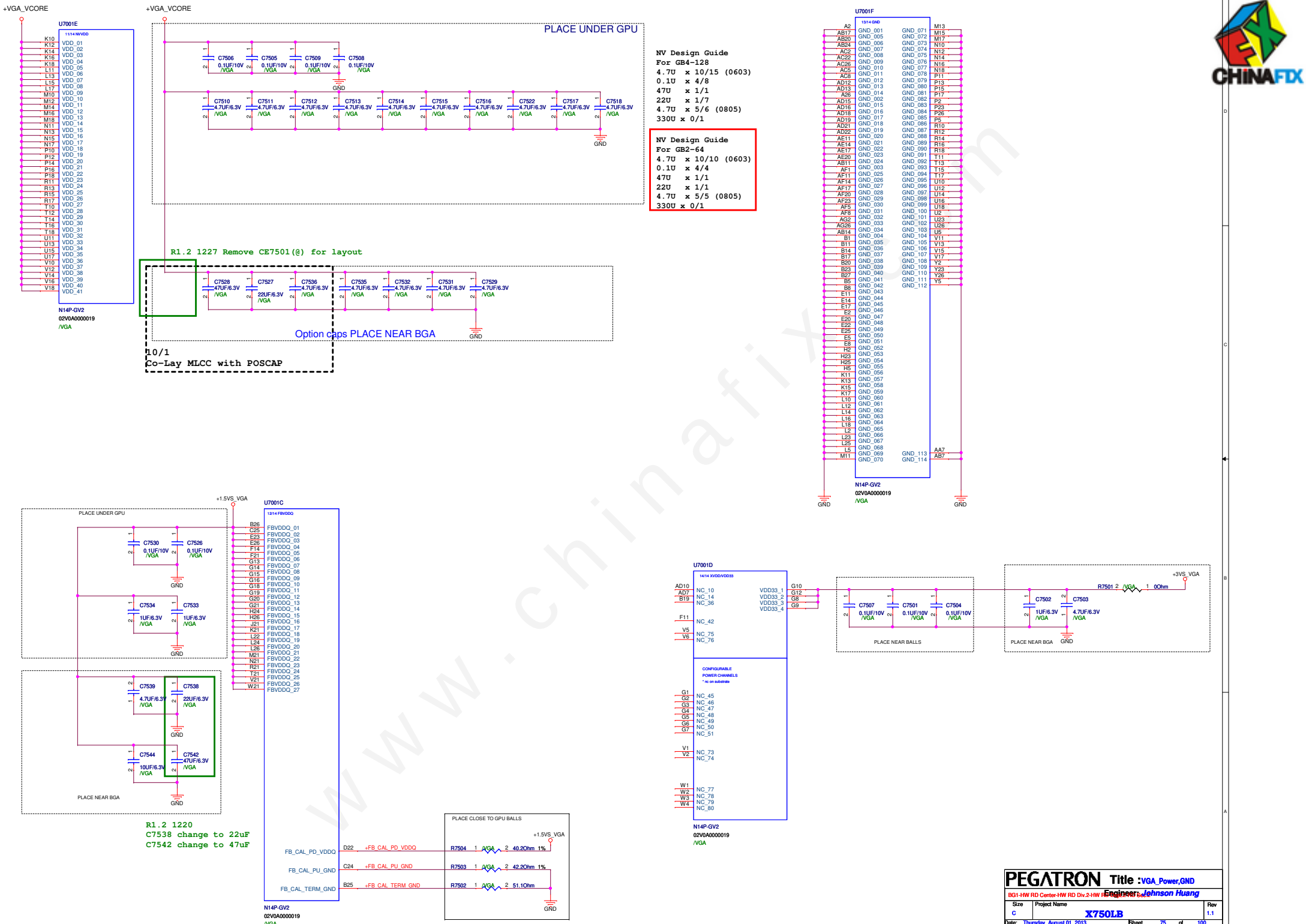
Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Sec.1

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 73 of 100


U7001L
GF117/GF119/GK208
NC_39
NC_41
E10
F10
ROM_CS#
ROM_SI
ROM_SO
ROM_SCLK
D12
B12
A12
C12
T7401
/VGA
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
D1
D2
E4
E3
D3
GF119
GF117 GK208
NC_37
C1
BUFRST#
D11
D10
R7402 2 /VGA 1 10KOhm
T7413 /VGA
NC_38
NC_40
E9
STRAP_REFGND
F6
MULTI_STRAP_REF0_GND
R7401
40.2KOhm
1%
/N14P-GV2/GS
/VGA
T7411
T7412
F4
F5
NC_43
NC_44
N14P-GV2
02V0A0000019
/VGA
R1.1 1128 Modify R7401 connection from pin F5 to F6
Add T7411 & T7412
R1.1 1129
Add T7413
+3VS_VGA
R7410 45.3KOhm 1% /VGA
R7412 34.8KOhm 1% @
R7414 10KOhm 1% @
R7417 45.3KOhm 1% @
R7418 10KOhm 1% @
R7411 45.3KOhm 1% @
R7413 45.3KOhm 1% /VGA
R7415 15KOhm 1% /VGA
R7416 4.99KOhm 1% /VGA
R7419 45.3KOhm 1% /VGA
R7404 5.1KOhm 1% @
R7405 4.99KOhm 1% /VGA
R7406 4.99KOhm 1% /VGA
R7407 15KOhm 1% /VGA
Hynix 4G
R7408 10KOhm 1% @
R7409 15KOhm 1% @
STRAP0(1,1,1,1 pu 45K)
USER[3:0]
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA -/-
0 0 0 1 XGA +/+
0 0 1 0 SXGA +/+
0 0 1 1 SXGA+ -/-
0 1 0 0 UXGA +/+
1 1 1 1 EDID N/A
GB4-128
STRAP1 (0,0,0,0 PD 5K)
3GIO_PADCFG[3:0]
3 2 1 0
0 0 0 0 Gen3 support
0 1 1 0 Gen1/ Gen2 only
others RESERVED
ROM_SO (1,0,0,0 PU 5K))
LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE
ROM_SCLK(1,0,0,0 PU 5K)
for GV2 QS
LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEX_PLL_EN_TERM
5K PU 1000 PD 0000
10K PU 1001 PD 0001
15K PU 1010 PD 0010
20K PU 1011 PD 0011
25K PU 1100 PD 0100
30K PU 1101 PD 0101
35K PU 1110 PD 0110
45K PU 1111 PD 0111
STRAP2 (0,0,1,0 PD 15K)
for GV2 QS
LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
STRAP3 (0,0,0,0 PD 5K)
LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
STRAP4 (0,0,0,1 PD 10K)
LOGICAL BIT
0 DP_PLL_VDD33V
1 PCIE_MAX_SPEED
2 PCIE_SPEED_CHANGE_GEN3
3 RESERVED
PCI_DEVID[3..0]
N14P-GV2 -->0X1292 ~ 0 0 1 0 --> pull down 15K
BINARY STRAP MODE MAPPING for N14M-GL
Pin Name Mapping
ROM_SCLK SMB_ALT_ADDR Pull down 10K
ROM_SI SUB_VENDOR Pull down 10K
ROM_SO VGA_DEVICE Pull down 10K
STRAP0 RAM_CFG[0]
STRAP1 RAM_CFG[1]
STRAP2 RAM_CFG[2]
STRAP3 RAM_CFG[3]
STRAP4 PCI_MAX_SPEED Pull down 10K
RAM_CFG[3:0]
Vendor Part Number Strap
Micron MT41J128M16JT-093G:K 0x1 (0001)
MT41J128M16JT-107G:K 0x1 (0001)
Hynix H5TQ4G63MFR-11C 0x3 (0011)
H5TQ4G63AFR-11C 0x4 (0100)
Samsung K4W2G1646E-BC1A 0x5 (0101)
K4W2G1646E-BC11 0x5 (0101)
Hynix H5TQ2G63DFR-N0C 0x6 (0110)
H5TQ2G63DFR-11C 0x6 (0110)
Samsung K4W4G1646B-HC11 0xB (1011)
Micron MT41K256M16HA-107G:E 0xD (1101)
1:Pull up 10k
0:Pull down 10k
ROM_SI RAMCONFIG (0,1,0,1 PD 30K)
Micron 256Mbx8
RAM_CFG[3:0]
Vendor Part Number Strap
Micron MT41K256M8DA-125:M 0x5 (0101) Pull down 30k
MT41K512M8RH-125:E 0x1 (0001) Pull down 10k
Hynix H5TC2G83EFR-PBA 0x6 (0110) Pull down 35k
H5TC4G83AFR-PBA 0x2 (0010) Pull down 15k
R1.2 0107 NV change strapping of Hynix 4G
MULTI-LEVEL MODE STRAPPING for N14P-GV2/GS
R1.2 0102 Add R7403,R7422,R7426,Q7409 for NV GC6 function
+3VS
R7422 10KOhm /VGA
Q7409 IRLML5103PBF 07V040000058 /VGA
Q7408A UM6K1N /VGA
R7426 10KOhm /VGA
GPU_FB_CLAMP
VGA_PWRON
FB_CLAMP_MON
R7403 10KOhm /VGA
U7001N
8/14 MISC1
SMB_CLK_VGA
SMB_DAT_VGA
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
R7425B 2.2KOhm /VGA
R7425A 2.2KOhm /VGA
RN7424A 2.2KOhm
RN7424B 2.2KOhm
RN7424C 2.2KOhm
RN7424D 2.2KOhm
Q7405A UM6K1N /VGA
Q7405B UM6K1N /VGA
SMB1_CLK
SMB1_DAT
THERMDN
THERMDP
VGA_THERMDN
VGA_THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
R7424 10KOhm /VGA
FB_CLAMP_MON
FB_CLAMP_TGL_REQ# VGA
VGA_OVERTEMP# R_GPIO8
THERM_ALERT# GPIO9
AC_BATT#
VGA_VID
VGA_PSI
VPS
R7434 0Ohm /N14P-GV2/GS
R7435 10KOhm /N14P-GV2/GS
R7420 10KOhm
SP7401
R0402 VGA_OVERTEMP# R
R0402 THERM_ALERT#
R7421 10KOhm /VGA
R7422A 10KOhm /VGA
R7422B 10KOhm /VGA
R1.2 1228 Set R7432 un-mount
R7432 10KOhm
PEX_RST#
C7402 4.7UF/6.3V
Q7403 2N7002 /VGA
VGA_THERM#
Pull high +3VS at system
R1.0 1101 For GPU Throttle
R7423 10KOhm /VGA
Q7401B UM6K1N /VGA
Q7401A UM6K1N /VGA
THRO_GPU
R1.2 0102 Modify R7428 for GC6 function NV Suggestion
R7428 10KOhm /VGA
Q7408B UM6K1N /VGA
FB_CLAMP_TGL_REQ#
R1.2 0102 PU 10K ohm move to EC side
C7401 4.7UF/6.3V /VGA
Q7402 2N7002 /VGA
THERM_ALERT#
VGA_ALERT#
R1.0 1031 ADD VGA_ALERT# (Thermal sensor to GPU)
PEGATRON
Title : VGA_GPIO,STRAP
Engineer: Johnson Huang
Size C
Project Name X750LB
Rev 1.1
Date: Thursday, August 01, 2013
Sheet 74 of 100



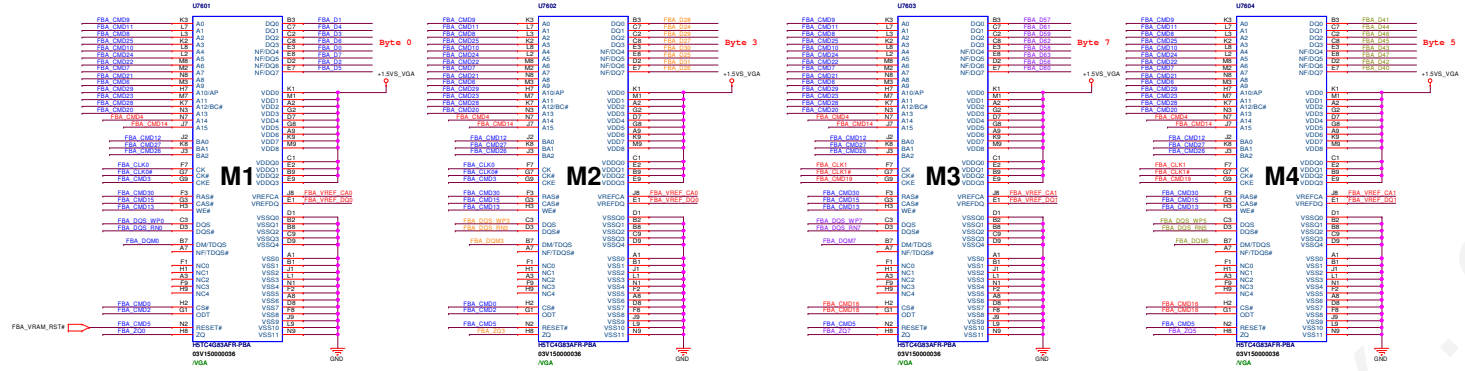
www.chinafix.com

PEGATRON	Title : VGA_Power,GND	
BG1-HW RD Center-HW RD Div.2-HW RD Sec.1	Engineer: Johnson Huang	
Size: C	Project Name: X750LB	Rev: 1.1
Date: Thursday, August 01, 2013	Sheet 75 of 100	

VRAM CH A

Mode D Command Mapping

TOP SIDE --- M1, M2, M3, M4



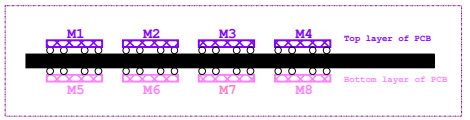
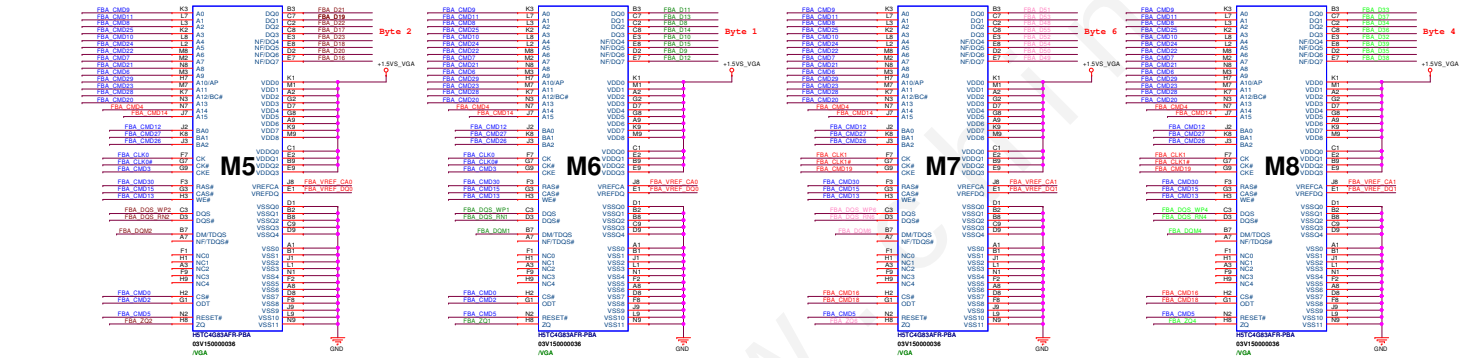


Table 29. Combined/Separate Memory FBVDD/Q Decoupling DDR3 x16 with DRAM on One Side

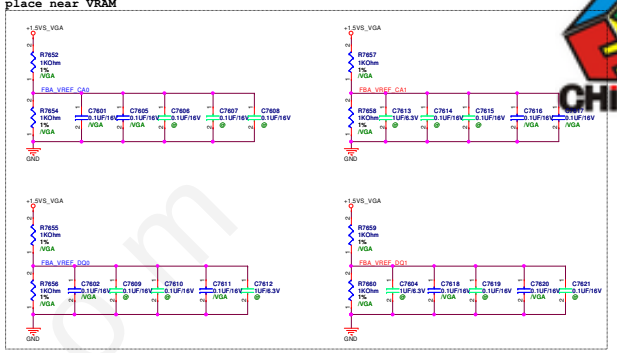
Capacitor	Type		Population* for Combined FBVDD/FBVDDQ	Population* for Separate FBVDDQ	Population* for Separate FBVDD	Location
0.1 µF	X7R	0402	2	4	2	Under DRAM
1.0 µF	X7R	0603	4	3	1	Under DRAM

*Per memory chip

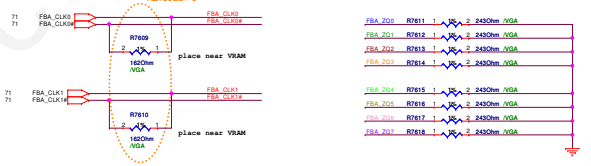
BOTTOM SIDE --- M5, M6, M7, M8

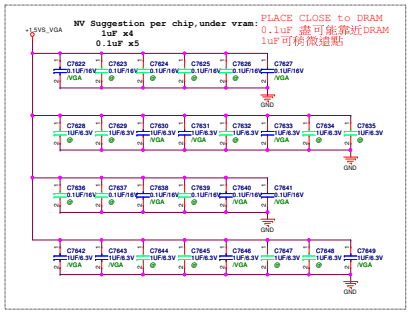


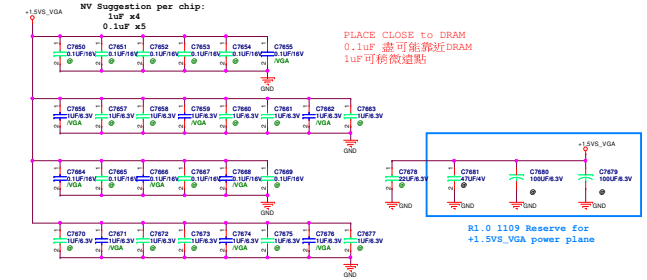
place near VRAM



NVIDIA Spec. 建議值為160 ohm







www.chinafix.com

PEGATRON Title : VGA_FBA_HYNIX DDR3 [31-2]
SGI-HW RD Center-HW RD Div.2-HW Engineer: Johnson Huang
Size: D | Project Name: X750LB | Rev: 1.1
Date: Thursday, August 01, 2013 | Sheet 76 of 100

VRAM CH C

www.chinafix.com

R1.0
delete Ventura.

www.chinafix.com

PEGATRON

Title : VGA_VENTURA_INA219

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-HW RD Sec.2

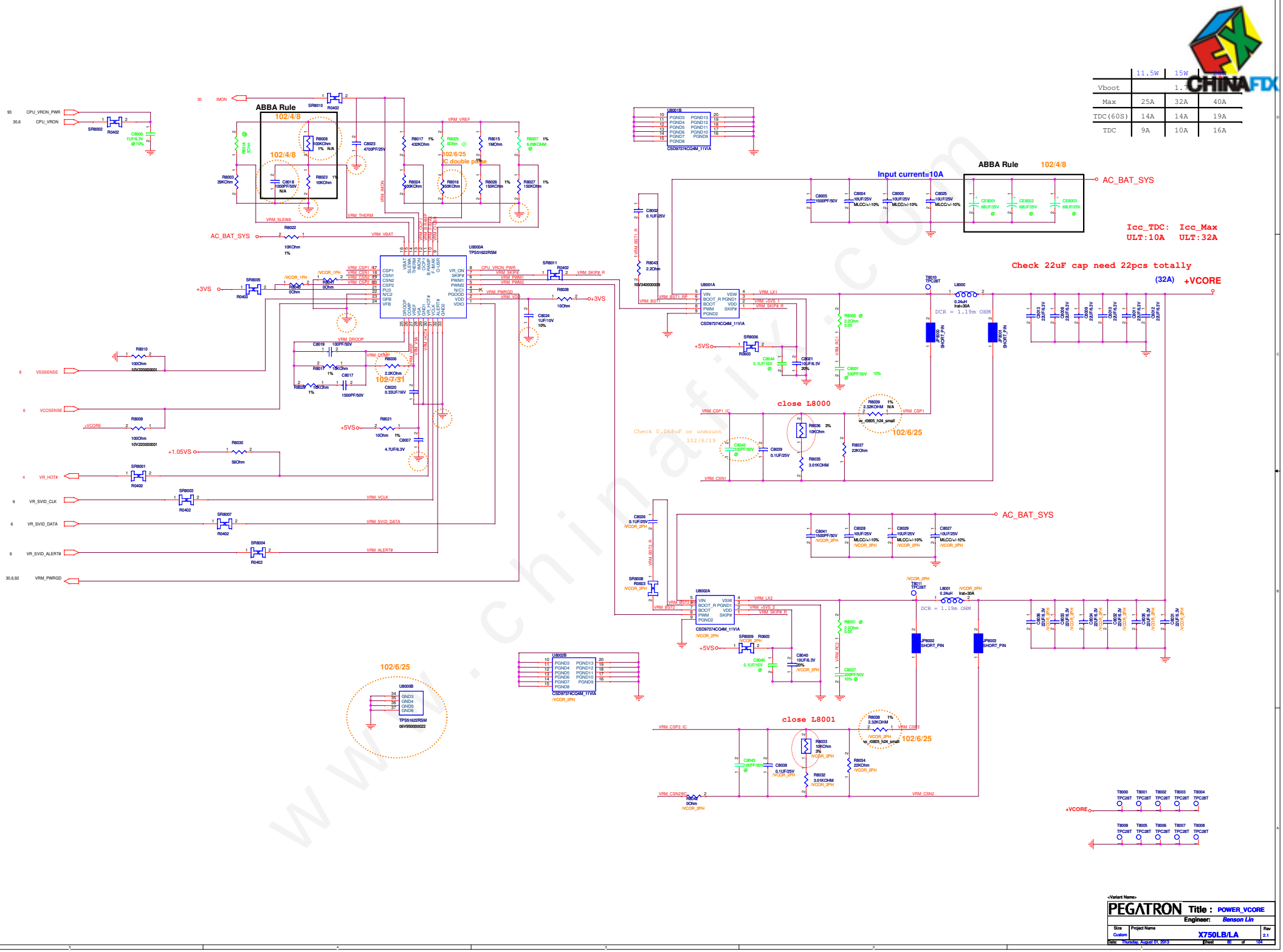
Size	Project Name	Rev
B	X750LB	1.1
	P/N <OrgAddr2>	

Date: Thursday, August 01, 2013 Sheet 78 of 100

R1.0
delete GB3-128 additional schematic.

www.chinafix.com

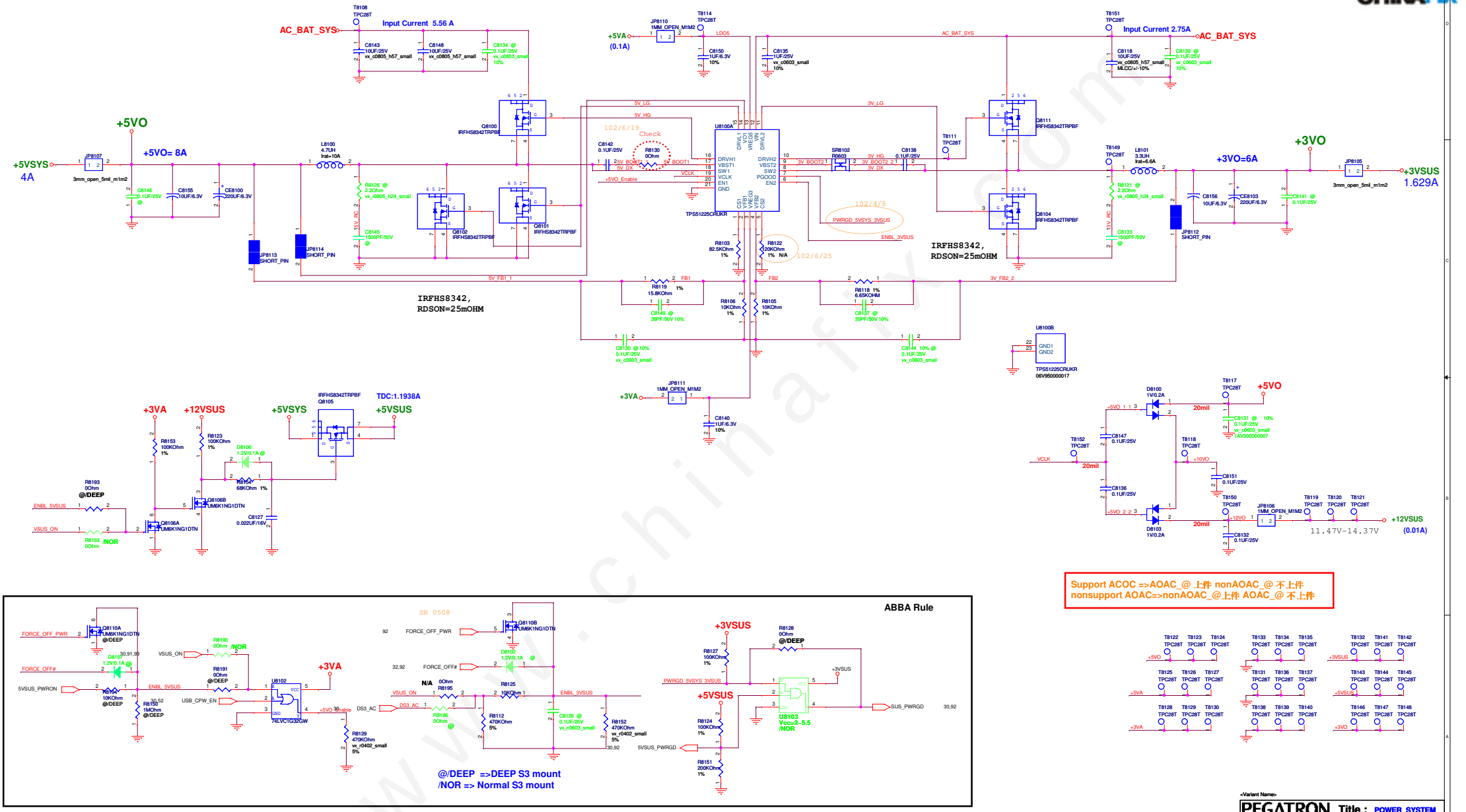
PEGATRON	Title : ADDITIOAL		
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2	Engineer: Johnson Huang		
Size: A	Project Name: X750LB		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, August 01, 2013	Sheet 79 of 100		



	11.5W	15W	
Vboot		1.7	
Max	25A	32A	40A
TDC(60S)	14A	14A	19A
TDC	9A	10A	16A

www.chinafix.com

+5VO & +3VO POWER SUPPLY



Support ACOC =>AOAC_@ 上件 nonAOAC_@ 不上件
nonsupport AOAC=>nonAOAC_@上件 AOAC_@ 不上件

www.chinafix.com

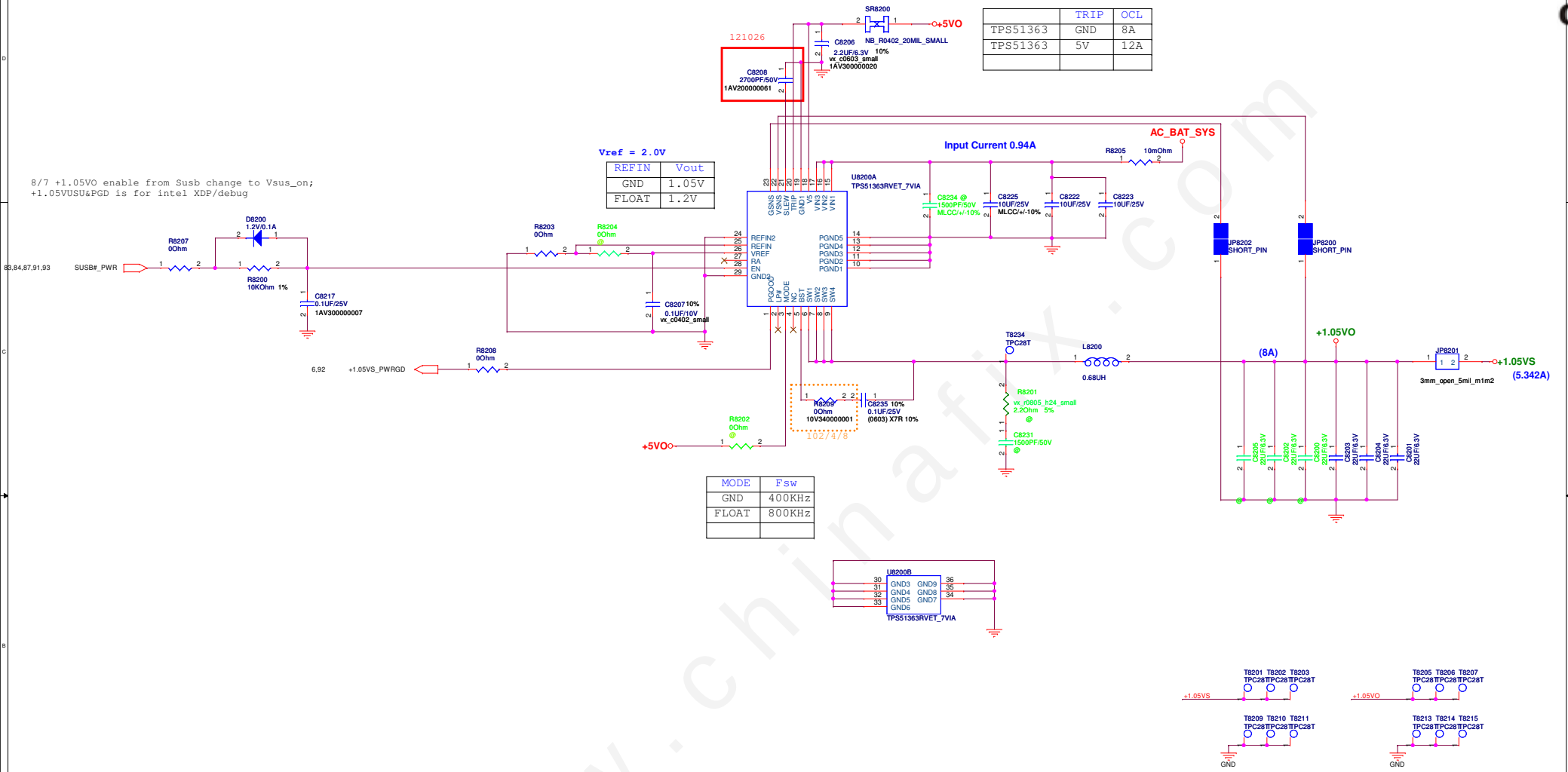
<variant_name>

PEGATRON Title : POWER_SYSTEM
Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 81 of 99

+1.05VS POWER SUPPLY



www.chinafix.com

CHINAFIX

<variant_name>

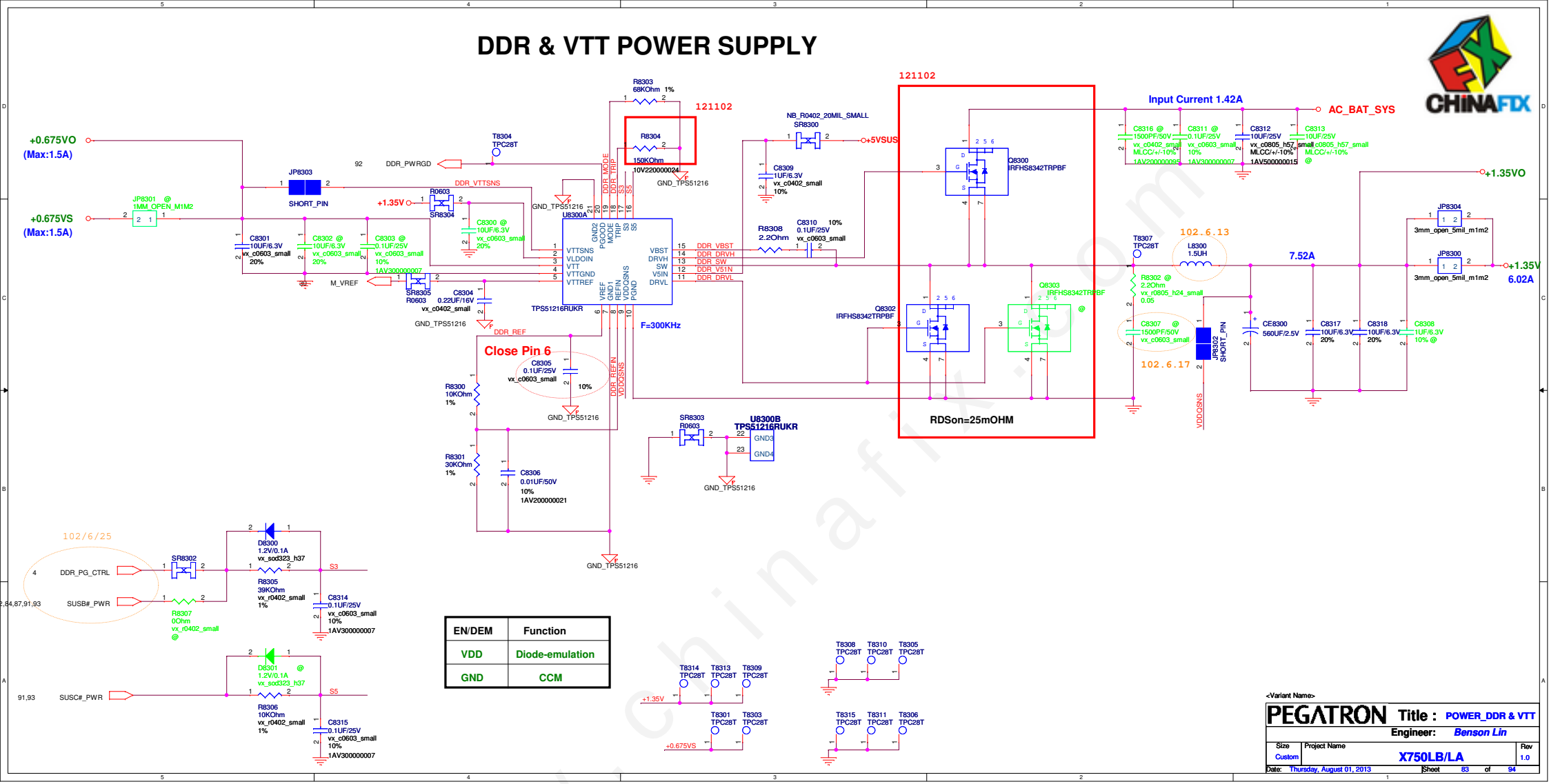
PEGATRON Title : POWER_+1.05VS

Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 82 of 94

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

PEGATRON Title : POWER_DDR & VTT

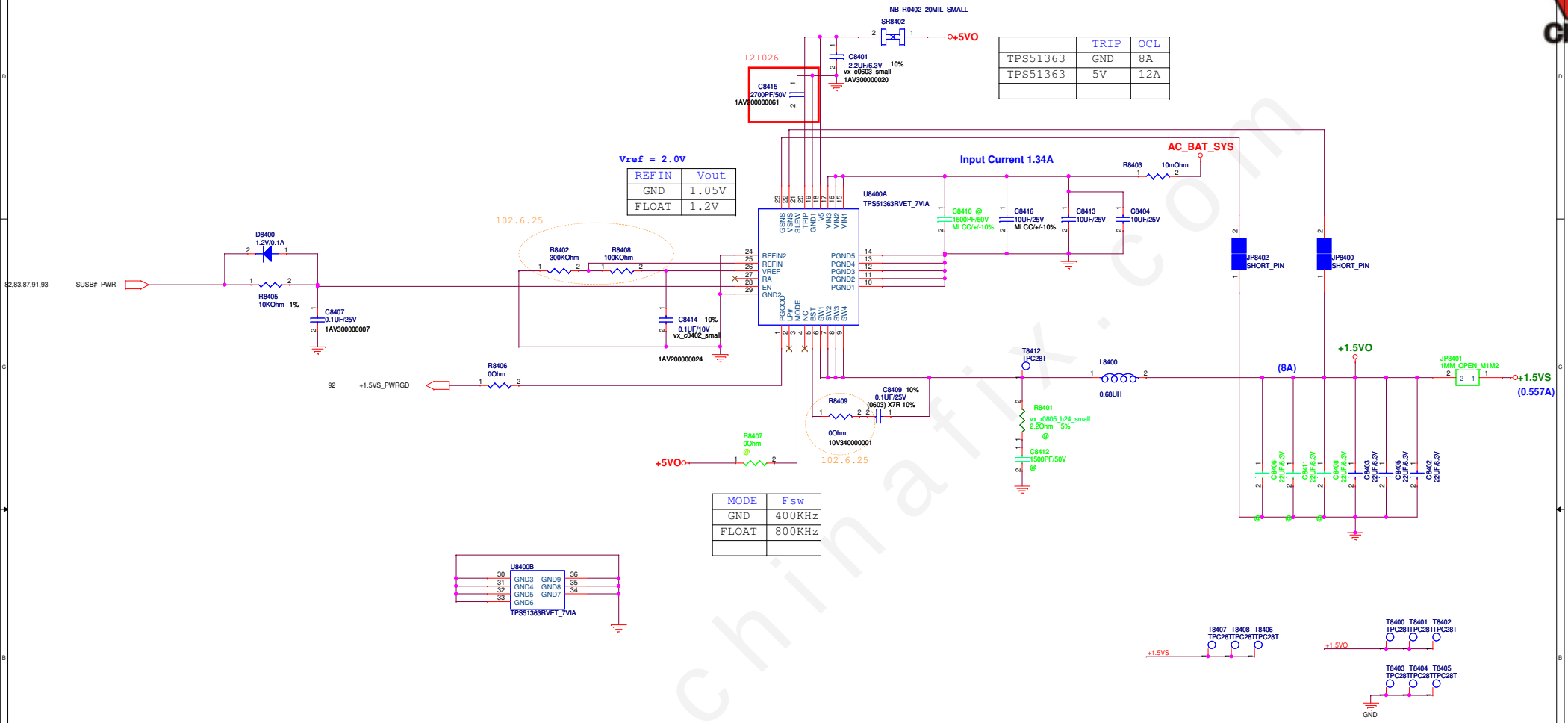
Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 83 of 94

www.chinafix.com

+1.5VS POWER SUPPLY



www.chinafix.com

<Variant Name>

PEGATRON Title : POWER_1.5VS

Engineer: Benson Lin

Size	Project Name	Rev
C	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 84 of 94

www.chinafix.com

<Variant Name>

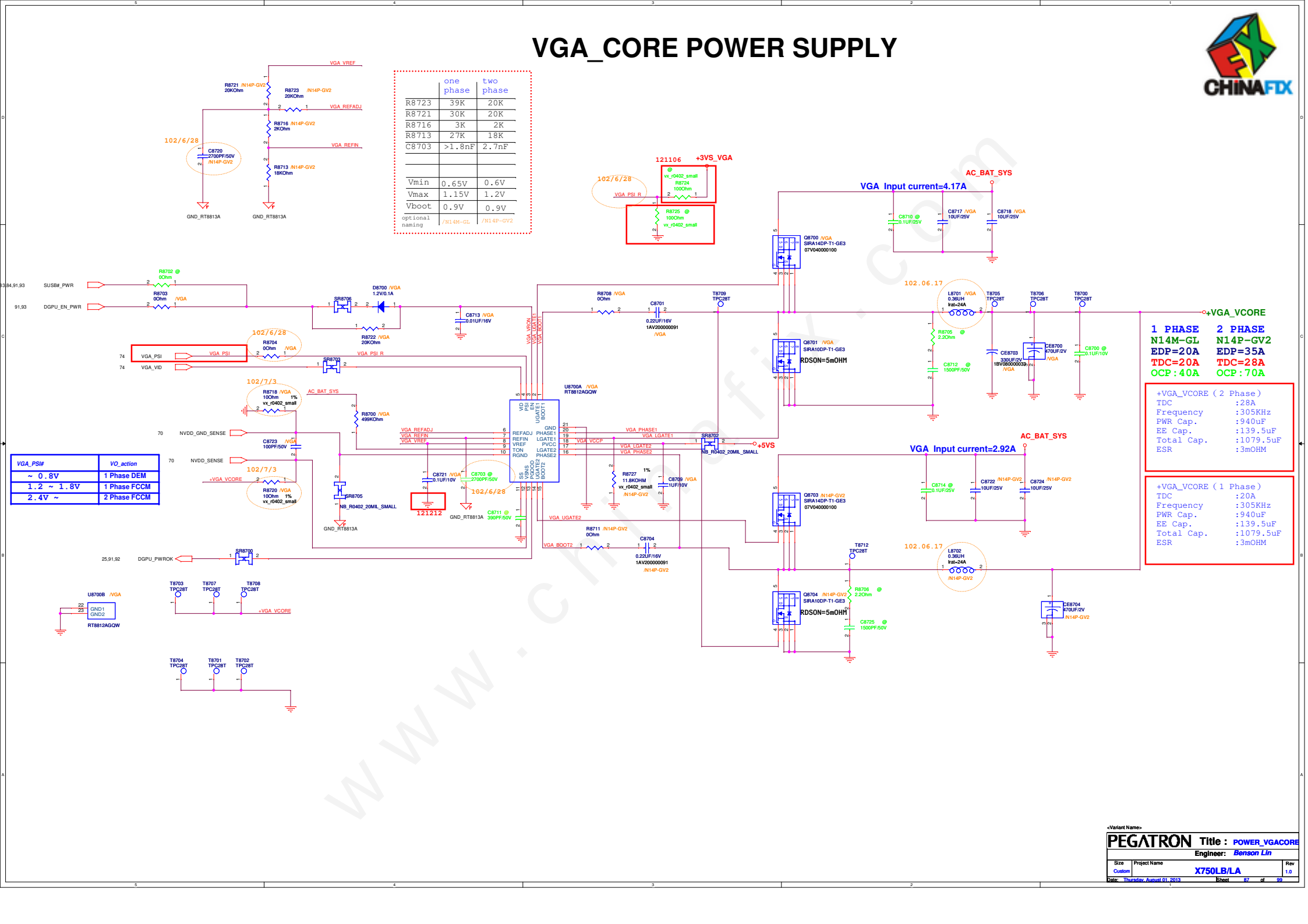
PEGATRON Title : POWER_1.8VS

Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 85 of 94

VGA_CORE POWER SUPPLY



www.chinafix.com

<Variant Name>

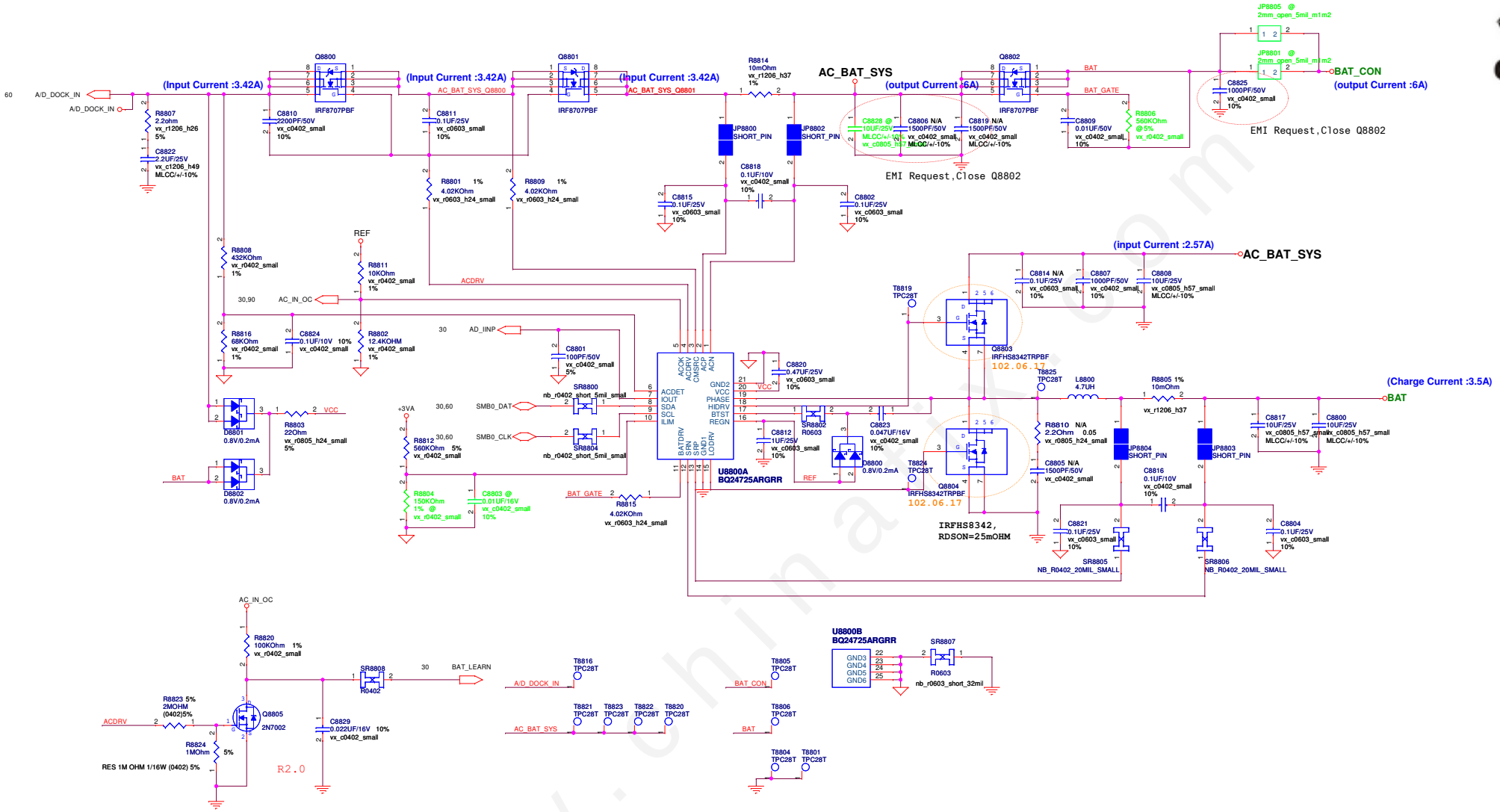
PEGATRON Title : POWER_VGACORE

Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 87 of 99

BATTERY CHARGER



www.chinafix.com

<Variant Name>

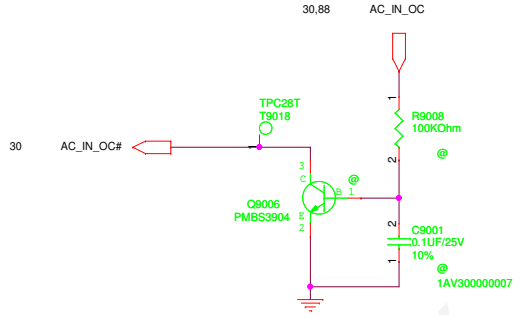
PEGATRON Title : POWER_CHARGER

Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 88 of 94

ADAPTER IN DETECT

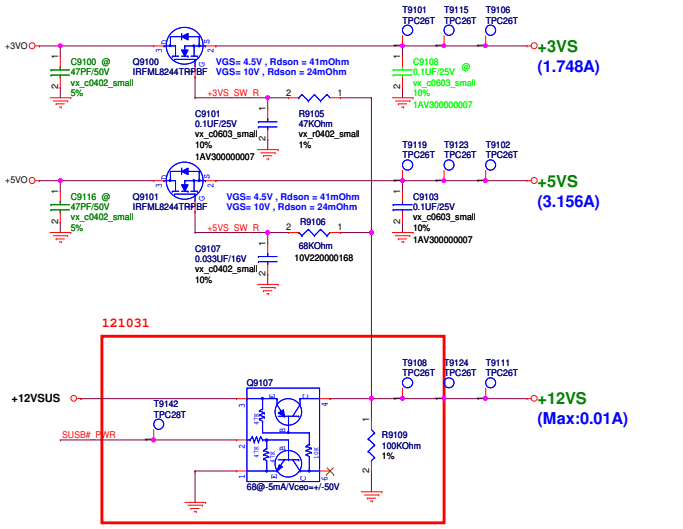


www.chinafix.com

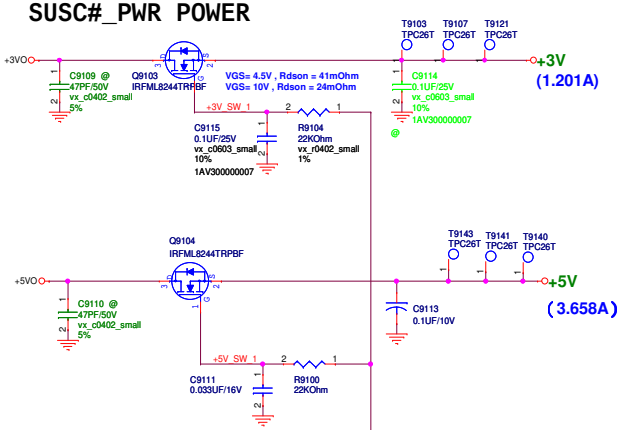
<Variant Name>

PEGATRON	Title : POWER_DETECT	
	Engineer: Benson Lin	
Size: Custom	Project Name: X750LB/LA	Rev: 1.0
Date: Thursday, August 01, 2013	Sheet 90 of 99	

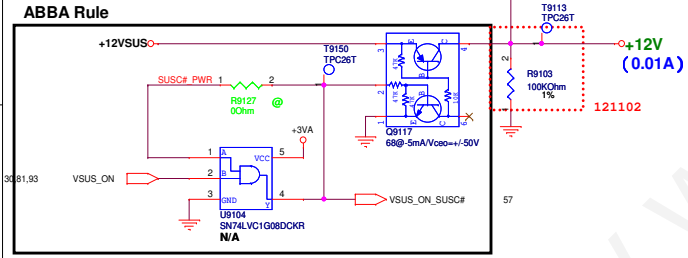
SUSB#_PWR POWER



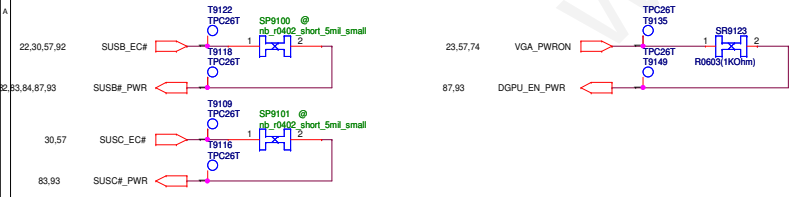
SUSC#_PWR POWER



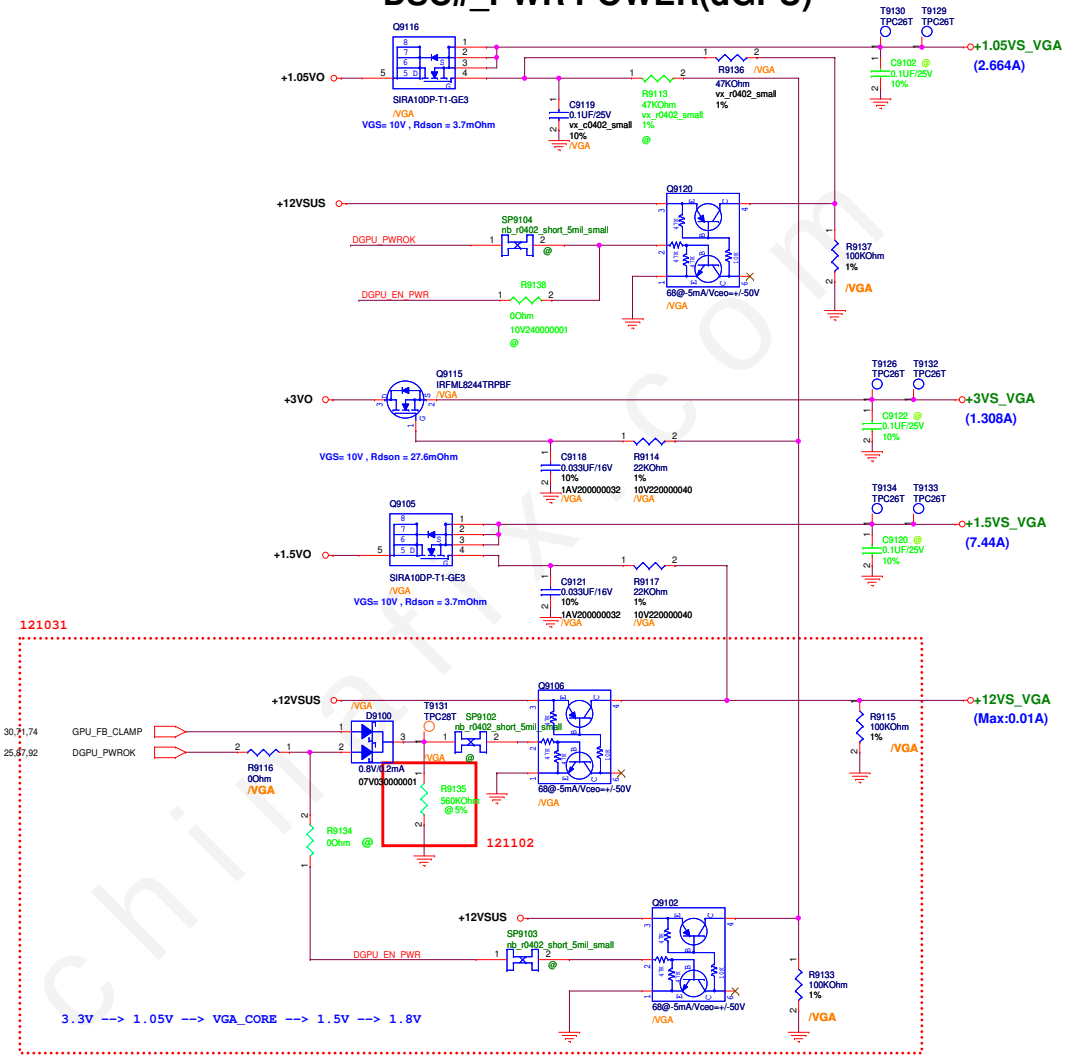
ABBA Rule

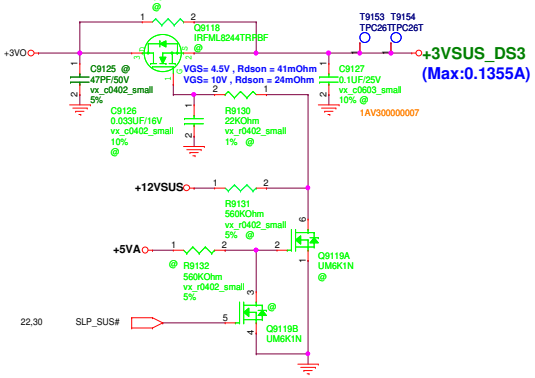


DSC_VGA_PWR POWER Control



DSC#_PWR POWER(dGPU)





<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

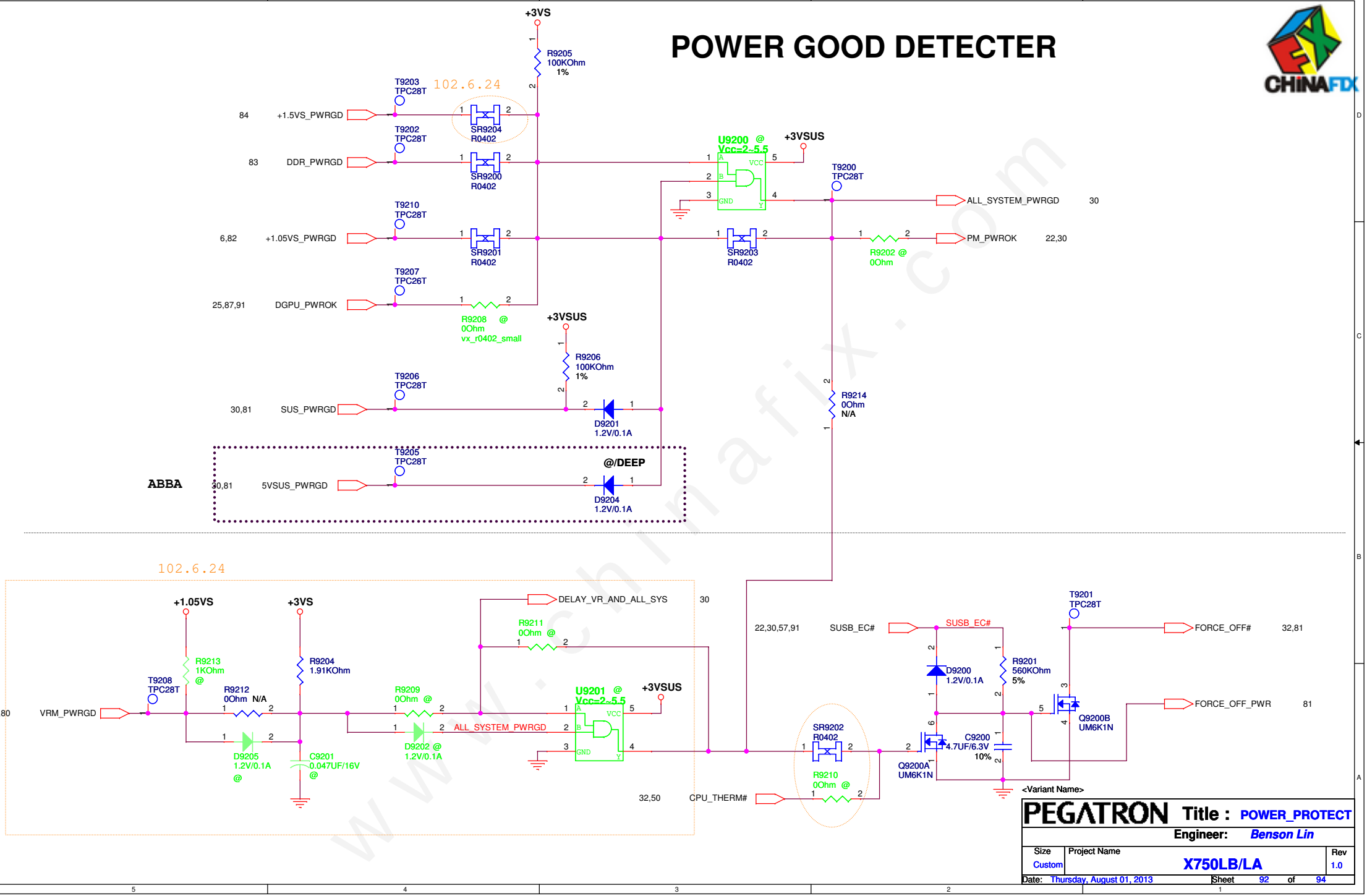
Engineer: Benson Lin

Size	Project Name	Rev
C	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 91 of 94

www.chinafix.com

POWER GOOD DETECTER



PEGATRON Title : POWER_PROTECT

Engineer: Benson Lin

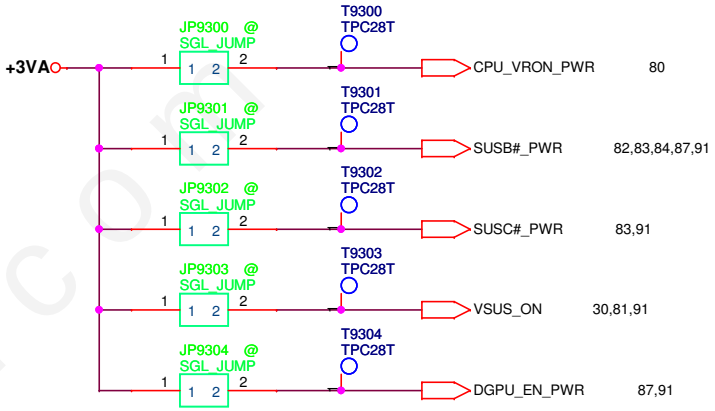
Size	Project Name	Rev
Custom	X750LB/LA	1.0

Date: Thursday, August 01, 2013 Sheet 92 of 94

www.chinafix.com

AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,84,87,88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	81,91
+3VA	+3VA	20,26,30,57,81,88,91
+5VO	+5VO	81,82,84,91
+3VO	+3VO	81,91
+1.05VO	+1.05VO	82,91
+12VSUS	+12VSUS	22,26,51,81,91
+5VSUS	+5VSUS	22,26,4,51,56,81,83
+3VSUS	+3VSUS	22,26,28,30,33,34,53,81,92
+12V	+12V	91
+3V	+3V	22,45,57,91
+12VS	+12VS	28,31,46,5,57,91
+5VS	+5VS	20,30,36,46,48,50,51,56,57,66,80,87,91
+3VS	+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+1.5VS	+1.5VS	26,53,57,84
+1.05VS	+1.05VS	25,26,32,46,57,6,80,82,92
+VCORE	+VCORE	6,80

FOR POWER TEST



www.chinafix.com

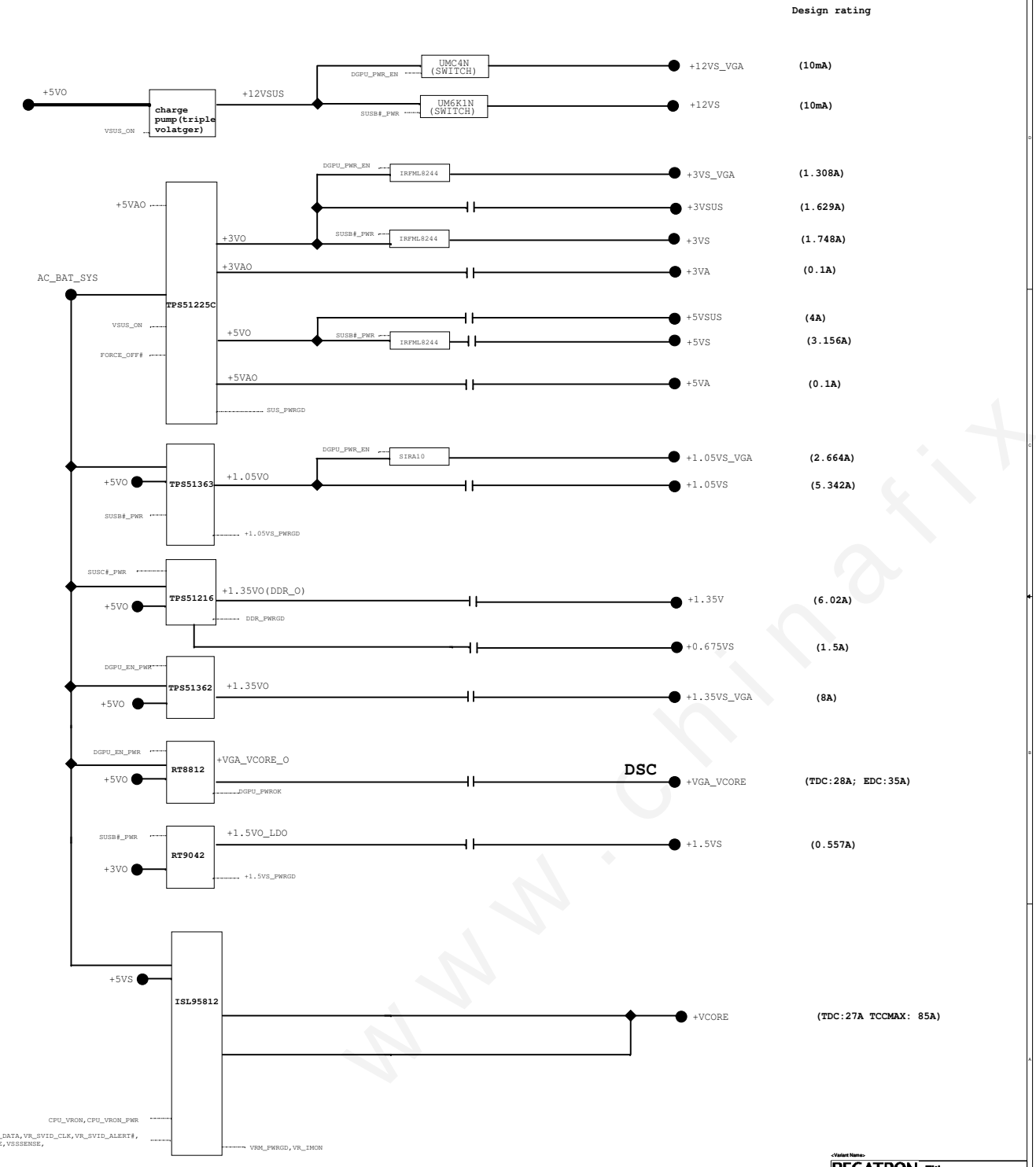
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Benson Lin

Size	Project Name	Rev
Custom	X750LB/LA	1.0

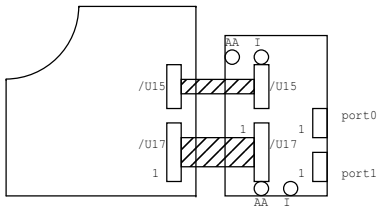
Date: Thursday, August 01, 2013 Sheet 93 of 94

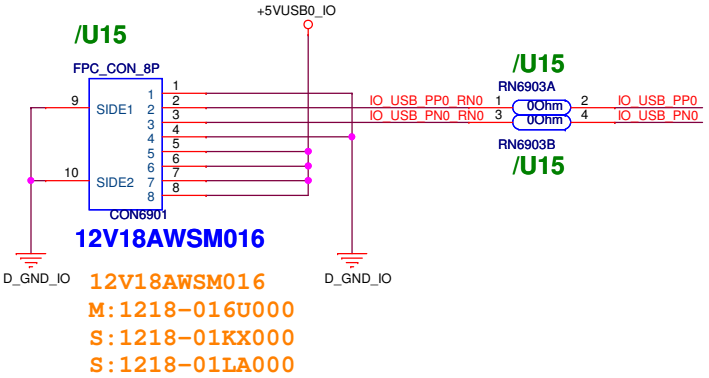


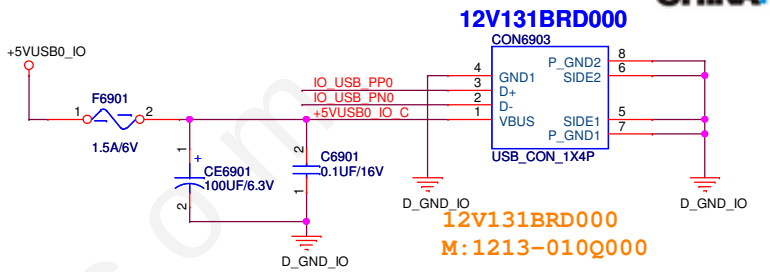
www.chinafix.com

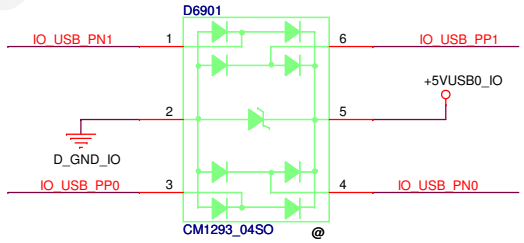
CHINAFIX

USB 2.0 USB 2.0 for 17"

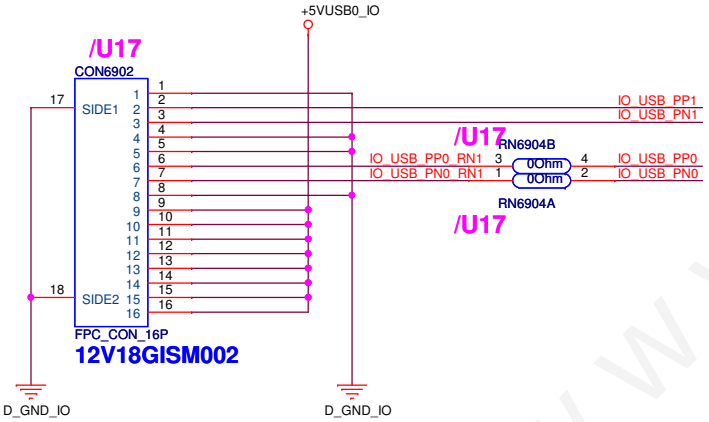


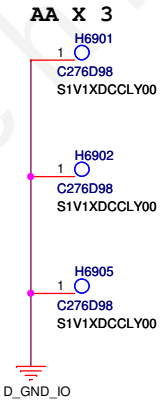


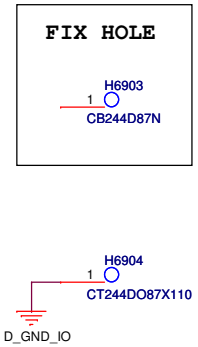


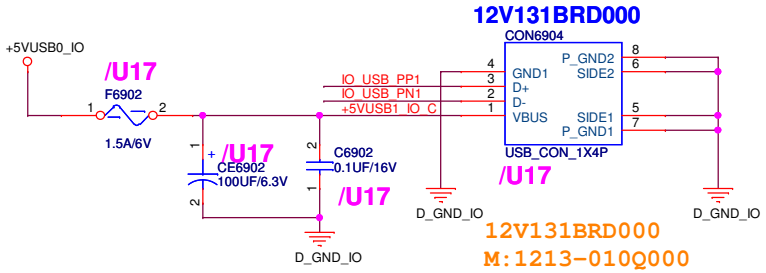


17" pin 5 對應15" pin1









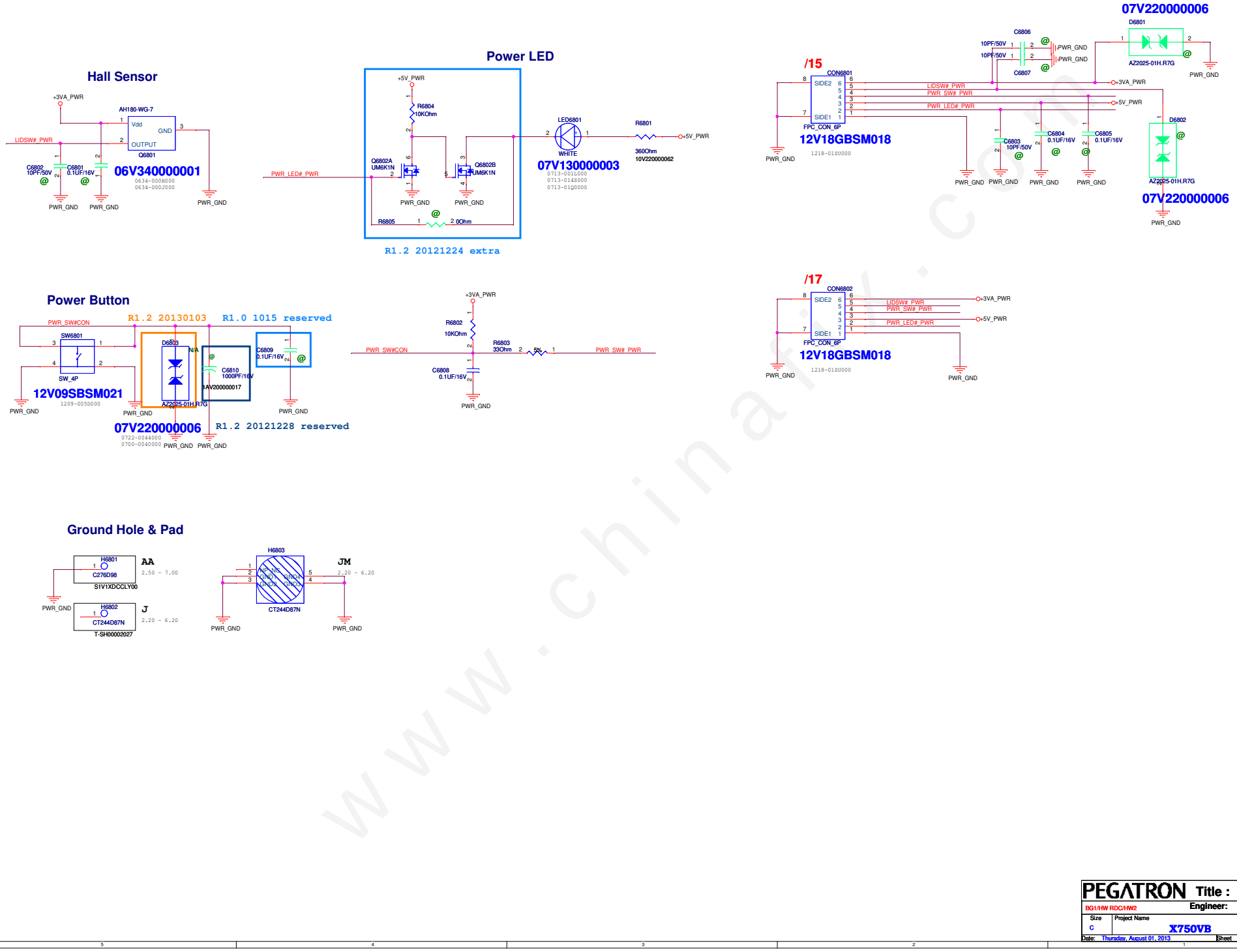
PEGATRON Title :IO

BG1/RDCenter Engineer: Osmand Fang

Size	Project Name	Rev
B	X750DP	1.0

Date: Thursday, August 01, 2013 Sheet 95 of 96

www.chinafix.com



www.chinafix.com

PEGATRON	Title : Power Switch Board	
BG1/HW RDC/HW2	Engineer: Abner Huang	
Size: C	Project Name: X750VB	Rev: 2.0
Date: Thursday, August 01, 2013	Sheet 96 of 96	

20130624

R2059, R2052, R2055, R3604 changed to SP2001, SP2002, SP2003, SP3601
Reserve F4501
Add C5113, C5111, C5127, C5128, C5123, C5124
Change H6514 for ME request
Delete H6521

20130625

R2057 change to SP2004
C7529, C7531, C7532, C7535, C7536 changed to 0805
C7679, C7680, C7681 changed to 3216 PosCap
Delete R2038-R2043
PCIE_RCOMP, PCIE_IREF PU from +1.05 to +1.05VS_AUSB3PLL
SATA_IREF PU from +1.05 to +1.05VS_ASATA3PLL
Mount R0411, R2026, R2223, U2201
Unmount R2202, U2002
Change R2123, R2124 to 0ohm
Add R1818, R1819, R1821, R1822, R1815, R1816, C1804, C1807, C1805

20130626

Add R4617-R4619
Change U4601 to VX PN
Delete T2539
U4601.3,4 connect from SMbus to I2C

20130627

Add R4620, R4621
Change SP5202, SP5203 to R5212, R5213
Reserve R5222, R5223
Change R2235 option to /nonINTEL_DS3
Reserve R3036, R3037, R0401, R0403, R0404, R2102
Change D6601, D4504

20130628

R2007 connect from +1.05VS to +1.05VS_ASATA3PLL
Reserve RN4601, RN4602, RN4603, Q4603, Q4602, U4602, U4603

20130630

Reallocate R4620, R4621 on the place between Q4602 and CON4602
Change RN4601 and RN4602 to 4.7kohm

20130701

Delete H6562

20130702

Change C7103 to 0603 size

20130703

Reserve R2238

20130709

Unmount C2611; Change R2615 to 0ohm
Reserve R3038, R3039

20130717

Reserve C3410, C3411
Change R2401 to 3.01Kohm
R2640, R2637 connect to DCPSUS

20130719

Change DS3_AC from GPG2 to GPI7

20130720

Delete SP3005

20130722

Change R3050 option to @
Mount R0502, R5111, R5112, R5113

20130724

Change all capacitors on GPU site to 0.1uF for PCIE GEN2

20130725

Unmount R4613, R4614

20130730

Add R2618, R2619

20130731

Reassign PCIE CLKREQ and add R2125, R2132, R2133

www.chinafix.com

CHINAFIX

PEGATRON Title : ****

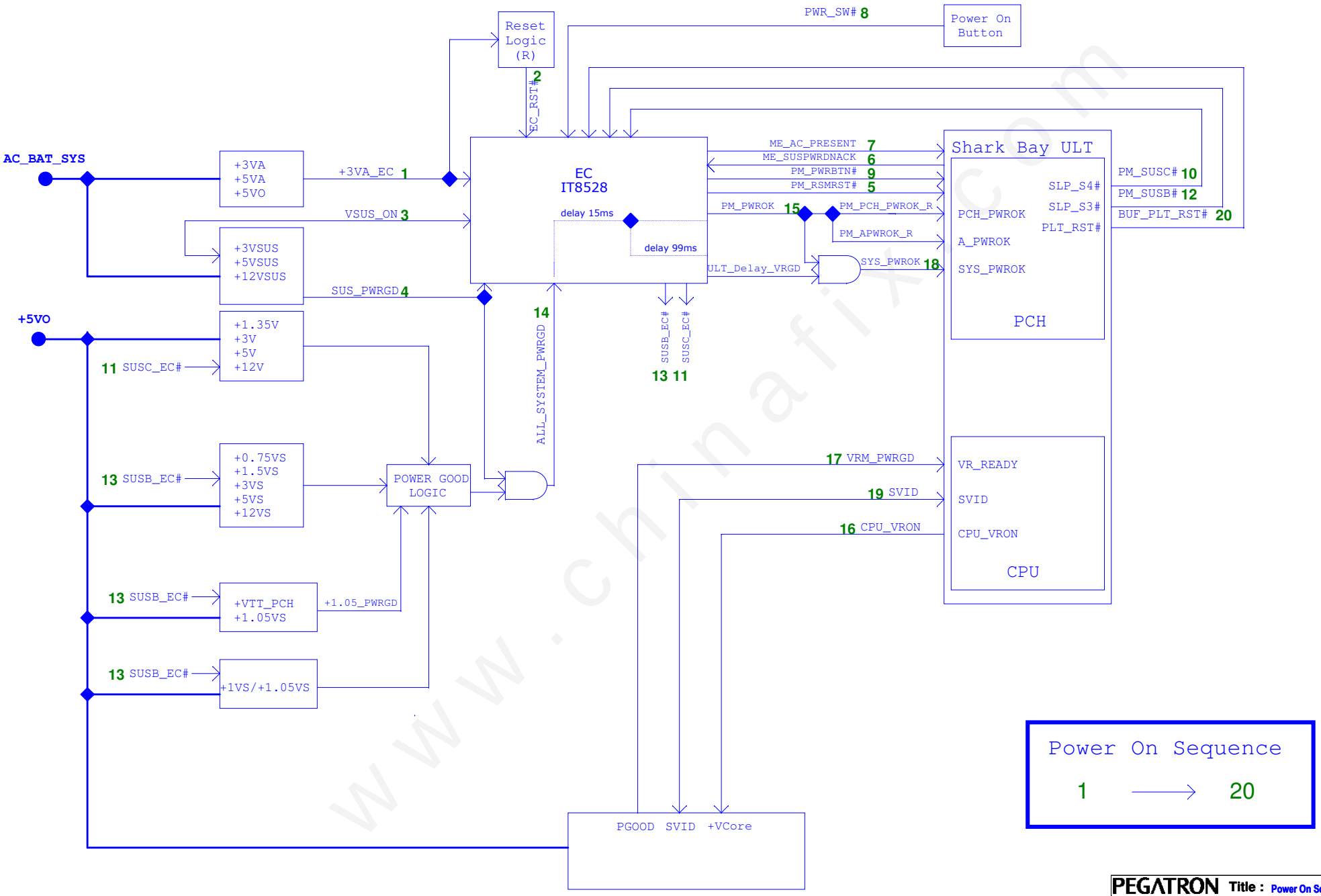
Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Sec.2

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 97 of 99

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



www.chinafix.com

CHINAFIX

PEGATRON Title : Power On Sequence

Engineer: Johnson Huang

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 98 of 99

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)

www.chinafix.com

PEGATRON Title : Power On Timing

Engineer: Johnson Huang

BG1-HW RD Center-HW RD Div.2-HW RD Sec.2

Size	Project Name	Rev
C	X750LB	1.1

Date: Thursday, August 01, 2013 Sheet 99 of 99